

Berry DG15 Discrete/UMA Schematics Document

Arrandale

Intel PCH

2009-10-12

REV : X00

DY :None Installed
UMA:UMA platform installed
DIS:DIS platform installed
Madisan:gDDR3 1GB platform installed
Colay :Manual modify BOM

<Core Design>



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover Page

Size
A3

Document Number

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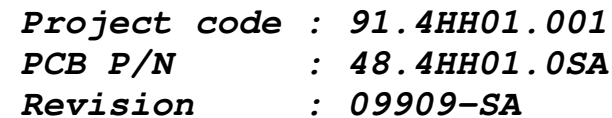
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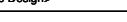
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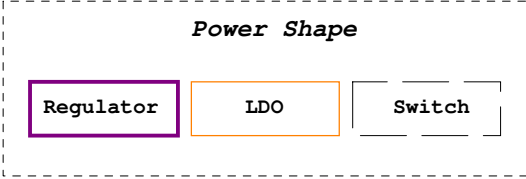
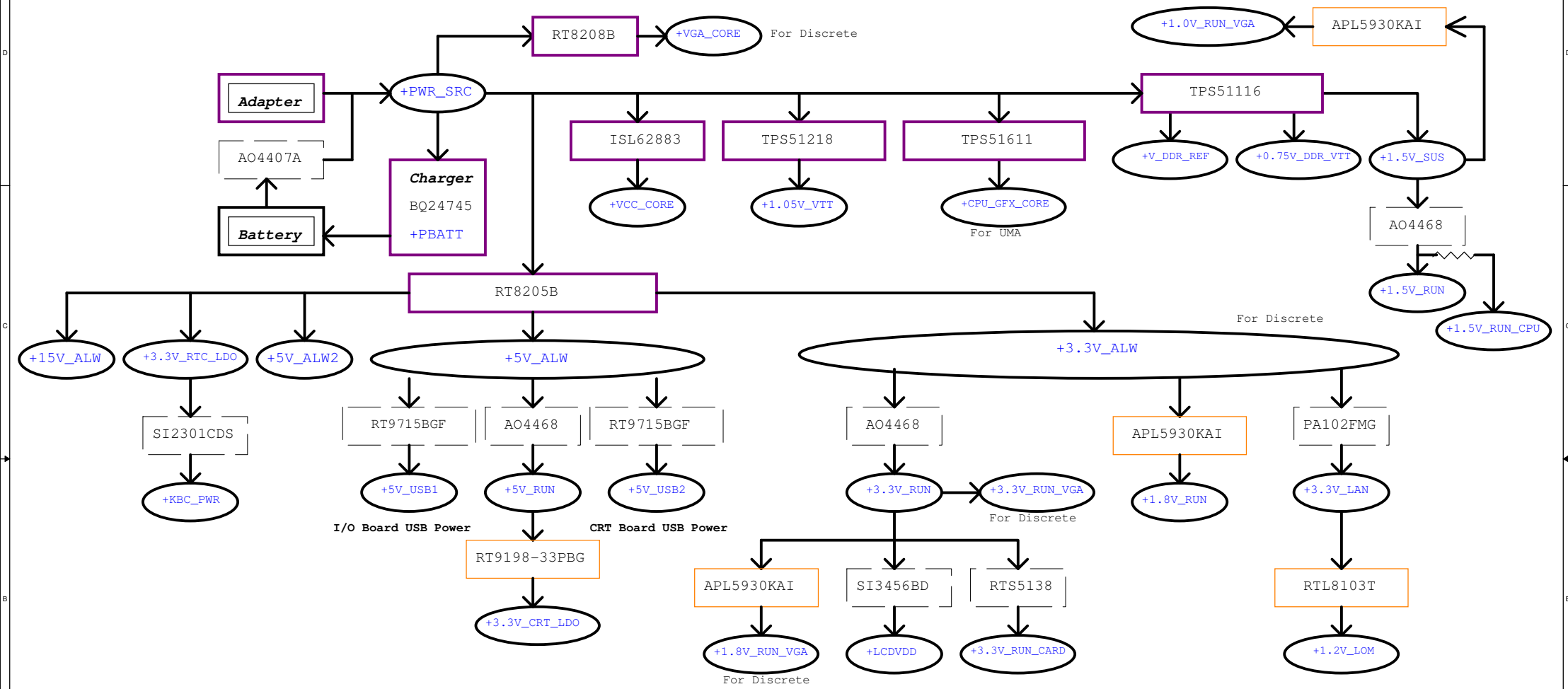
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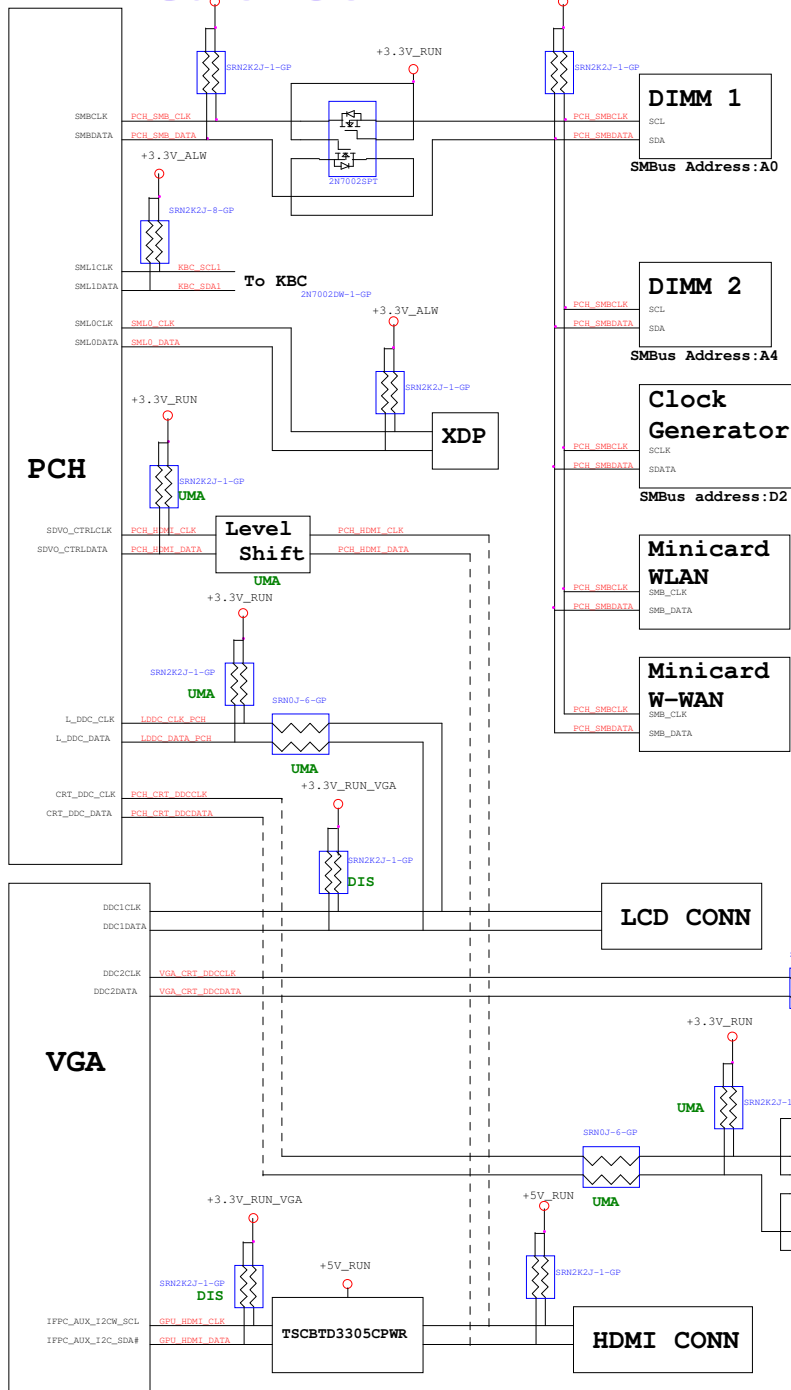
##OnMainBoard



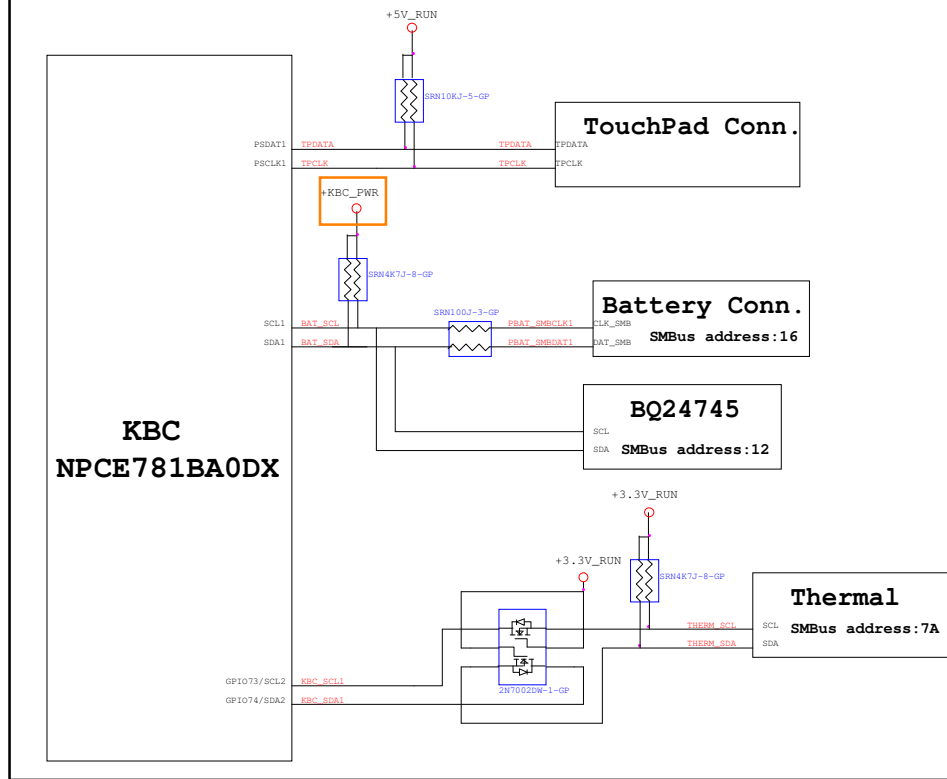
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		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	<i>Block Diagram</i>		
Size A3	Document Number Berry	Rev X00	
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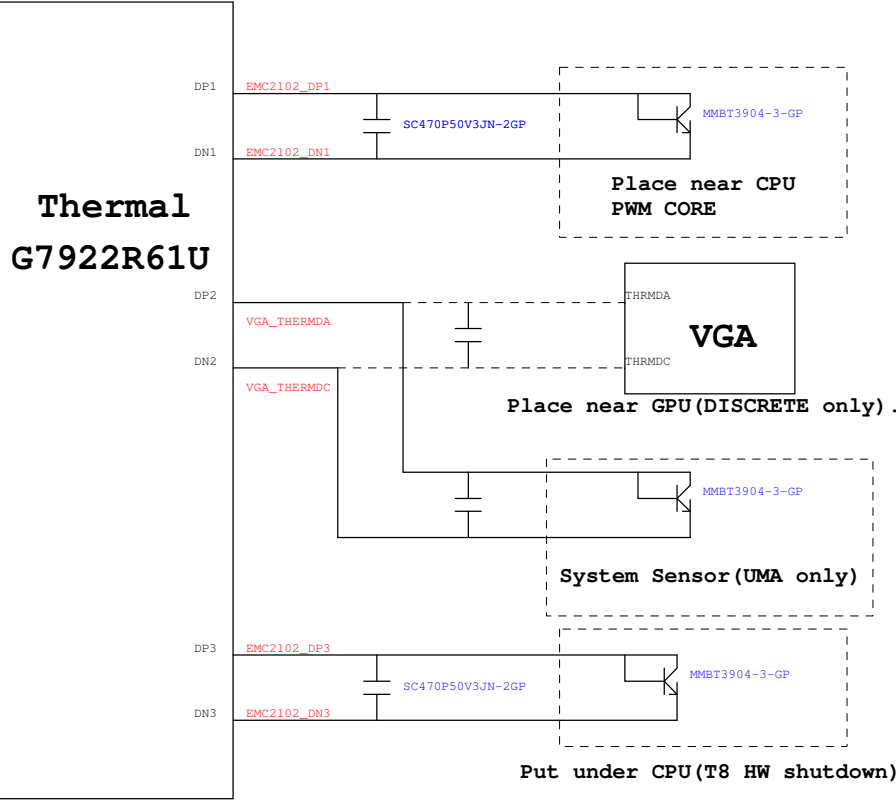
PCH SMBus Block Diagram



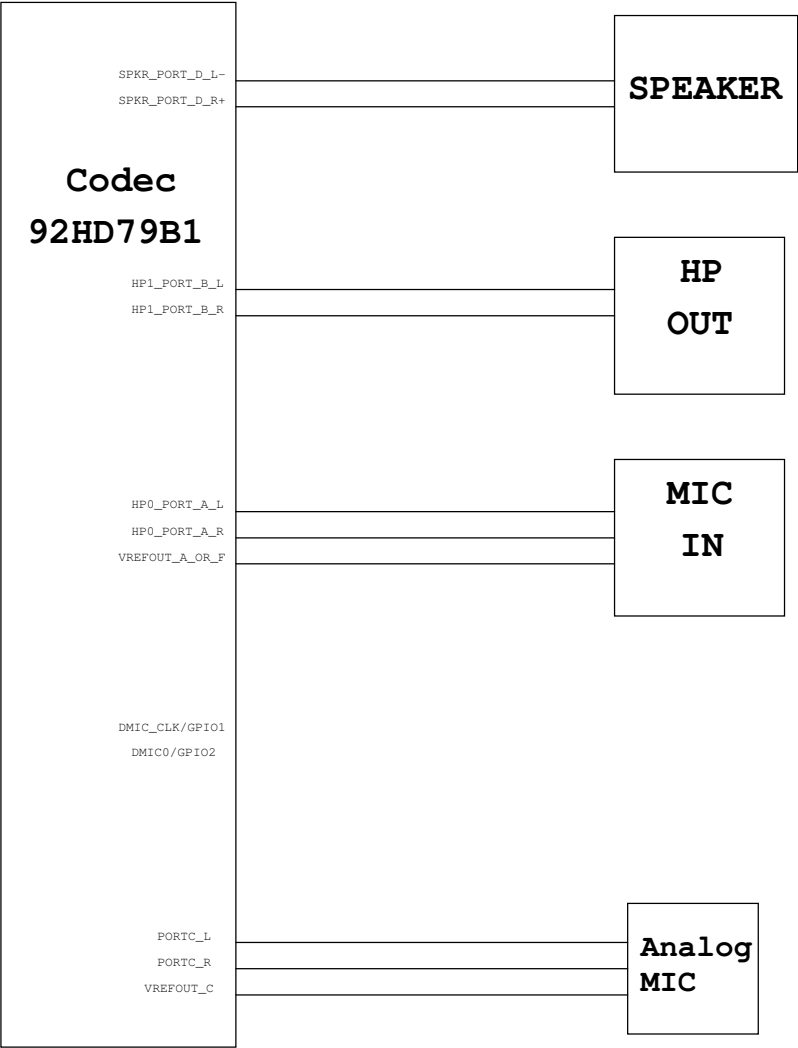
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



Calpella Schematic Checklist Rev.0_7

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#/GPIO51	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0) = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIE Routing

LANE1	RESERVED
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	W-WAN
LANE5	RESERVED
LANE6	RESERVED
LANE7	H55/HM55 no support
LANE8	H55/HM55 no support

USB Table

USB	
Pair	Device
0	USB2 (CRT Board)
1	USB3 (CRT Board)
2	WLAN (I/O Board)
3	RESERVED
4	CARD READER
5	BLUETOOTH
6	HM55 no support
7	HM55 no support
8	USB1 (I/O Board)
9	USB0 (I/O Board ESATA)
10	RESERVED
11	W-WAN (I/O Board)
12	RESERVED
13	CAMERA

SATA Table

SATA	
Pair	Device
0	HDD
1	ODD
2	HM55 no support
3	HM55 no support
4	ESATA
5	RESERVED

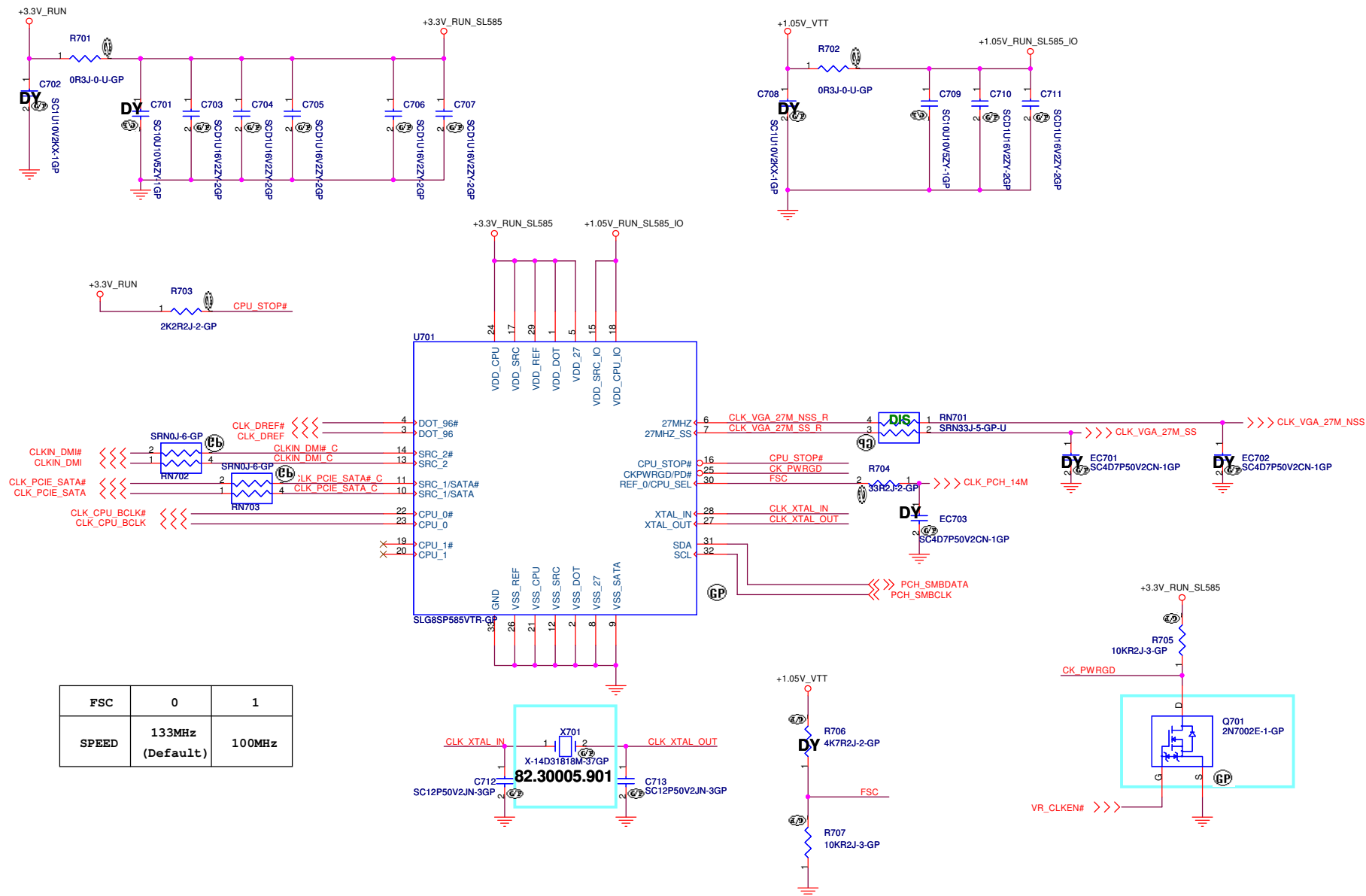
Processor Strapping

Calpella Schematic Checklist Rev.0_7

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

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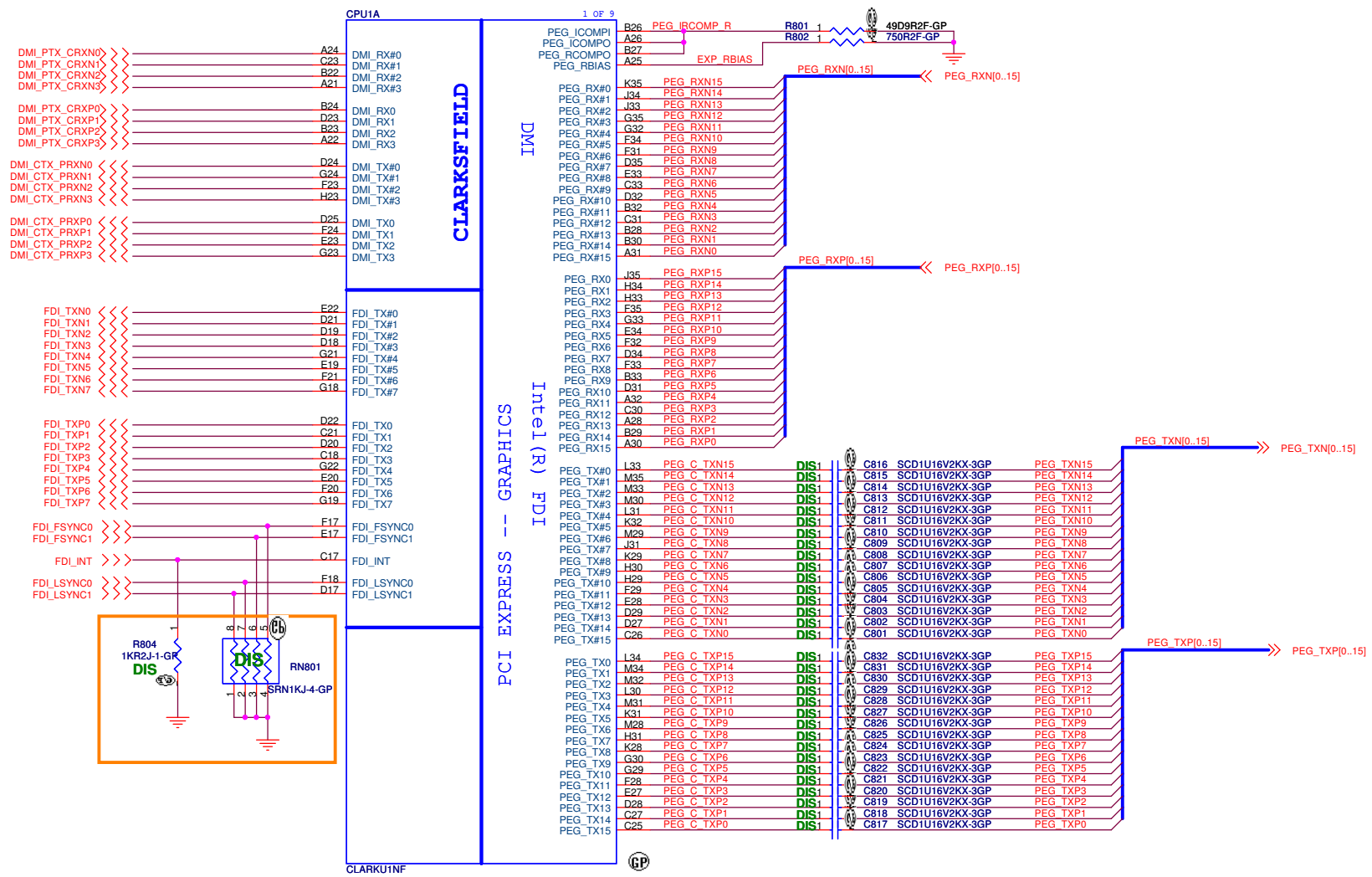
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Title			
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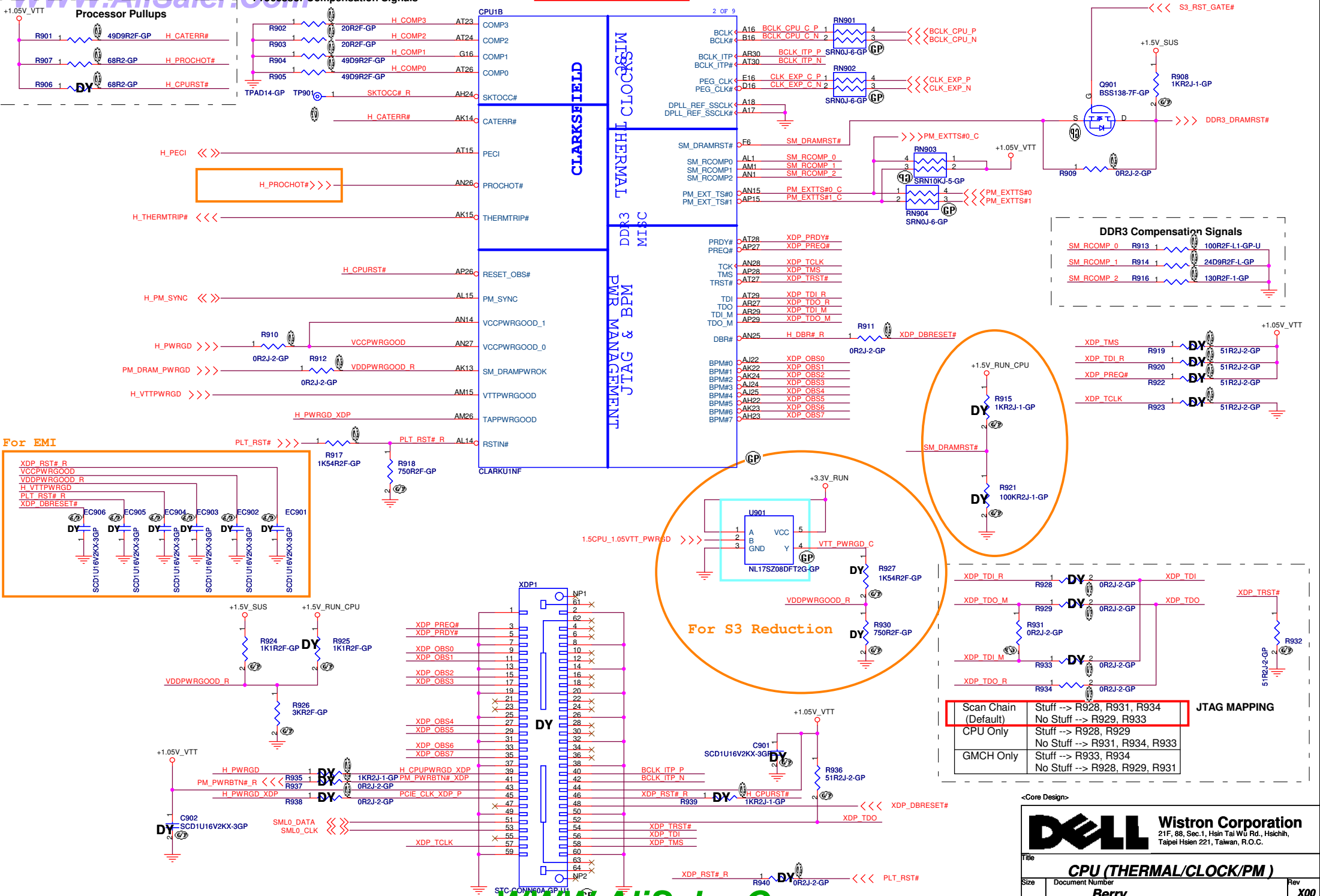


FSC	0	1
SPEED	133MHz (Default)	100MHz

SSID = CPU

WWW.AliSaler.Com





M_A_DQ[63..0] <<>> M_A_DQ[63..0]

M_A_DQ0 A10 SA_DQ0
M_A_DQ1 C10 SA_DQ1
M_A_DQ2 A7 SA_DQ2
M_A_DQ3 B10 SA_DQ3
M_A_DQ4 B10 SA_DQ4
M_A_DQ5 D10 SA_DQ5
M_A_DQ6 E10 SA_DQ6
M_A_DQ7 A8 SA_DQ7
M_A_DQ8 D8 SA_DQ8
M_A_DQ9 F10 SA_DQ9
M_A_DQ10 E6 SA_DQ10
M_A_DQ11 F7 SA_DQ11
M_A_DQ12 E9 SA_DQ12
M_A_DQ13 B7 SA_DQ13
M_A_DQ14 E7 SA_DQ14
M_A_DQ15 C6 SA_DQ15
M_A_DQ16 H10 SA_DQ16
M_A_DQ17 G8 SA_DQ17
M_A_DQ18 K7 SA_DQ18
M_A_DQ19 J8 SA_DQ19
M_A_DQ20 G7 SA_DQ20
M_A_DQ21 G10 SA_DQ21
M_A_DQ22 J7 SA_DQ22
M_A_DQ23 J10 SA_DQ23
M_A_DQ24 L7 SA_DQ24
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M_A_DQ28 L6 SA_DQ28
M_A_DQ29 K8 SA_DQ29
M_A_DQ30 N8 SA_DQ30
M_A_DQ31 P9 SA_DQ31
M_A_DQ32 AH5 SA_DQ32
M_A_DQ33 AE5 SA_DQ33
M_A_DQ34 AK6 SA_DQ34
M_A_DQ35 AK7 SA_DQ35
M_A_DQ36 AE6 SA_DQ36
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M_A_DQ41 AJ9 SA_DQ41
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M_A_DQ44 AK8 SA_DQ44
M_A_DQ45 AL7 SA_DQ45
M_A_DQ46 AK11 SA_DQ46
M_A_DQ47 AL8 SA_DQ47
M_A_DQ48 AN8 SA_DQ48
M_A_DQ49 AN10 SA_DQ49
M_A_DQ50 AR11 SA_DQ50
M_A_DQ51 AL11 SA_DQ51
M_A_DQ52 AM9 SA_DQ52
M_A_DQ53 AN9 SA_DQ53
M_A_DQ54 AT11 SA_DQ54
M_A_DQ55 AP12 SA_DQ55
M_A_DQ56 AM12 SA_DQ56
M_A_DQ57 AN12 SA_DQ57
M_A_DQ58 AM13 SA_DQ58
M_A_DQ59 AT14 SA_DQ59
M_A_DQ60 AT12 SA_DQ60
M_A_DQ61 AL13 SA_DQ61
M_A_DQ62 AP14 SA_DQ62
M_A_DQ63 AP14 SA_DQ63

M_A_BS0 <<>> AC3 SA_BS0
M_A_BS1 <<>> AB2 SA_BS1
M_A_BS2 <<>> U7 SA_BS2

M_A_CAS# <<>> AE1C SA_CAS#
M_A_RAS# <<>> AB3C SA_RAS#
M_A_WE# <<>> AE3C SA_WE#

CLARKSFIELD

DDR SYSTEM MEMORY A

SA_CK0 AA6 <<>> M_CLK_DDR0
SA_CK#0 AA7 <<>> M_CLK_DDR#0
SA_CKE0 P7 <<>> M_CKE0

SA_CK1 Y6 <<>> M_CLK_DDR1
SA_CK#1 Y5 <<>> M_CLK_DDR#1
SA_CKE1 P6 <<>> M_CKE1

SA_CS#0 AE2 <<>> M_CS#0
SA_CS#1 AE8 <<>> M_CS#1

SA_ODT0 AD8 <<>> M_ODT0
SA_ODT1 AF9 <<>> M_ODT1

SA_DM0 B9 M_A_DM0
SA_DM1 D7 M_A_DM1
SA_DM2 H7 M_A_DM2
SA_DM3 M7 M_A_DM3
SA_DM4 AG6 M_A_DM4
SA_DM5 AM7 M_A_DM5
SA_DM6 AN10 M_A_DM6
SA_DM7 AN13 M_A_DM7

SA_DQS#0 C9 M_A_DQS#0
SA_DQS#1 F8 M_A_DQS#1
SA_DQS#2 J9 M_A_DQS#2
SA_DQS#3 AN9 M_A_DQS#3
SA_DQS#4 AH7 M_A_DQS#4
SA_DQS#5 AK9 M_A_DQS#5
SA_DQS#6 AP11 M_A_DQS#6
SA_DQS#7 AT13 M_A_DQS#7

SA_DQS0 C8 M_A_DQS0
SA_DQS1 F9 M_A_DQS1
SA_DQS2 H9 M_A_DQS2
SA_DQS3 M9 M_A_DQS3
SA_DQS4 AH8 M_A_DQS4
SA_DQS5 AK10 M_A_DQS5
SA_DQS6 AN11 M_A_DQS6
SA_DQS7 AR13 M_A_DQS7

SA_MA0 Y3 M_A_A0
SA_MA1 W1 M_A_A1
SA_MA2 AA8 M_A_A2
SA_MA3 AA9 M_A_A3
SA_MA4 V1 M_A_A4
SA_MA5 AA9 M_A_A5
SA_MA6 V8 M_A_A6
SA_MA7 T1 M_A_A7
SA_MA8 Y9 M_A_A8
SA_MA9 U6 M_A_A9
SA_MA10 AD4 M_A_A10
SA_MA11 T2 M_A_A11
SA_MA12 U3 M_A_A12
SA_MA13 AG8 M_A_A13
SA_MA14 T3 M_A_A14
SA_MA15 V9 M_A_A15

M_B_DQ[63..0] <<>> M_B_DQ[63..0]

M_B_DQ0 B5 SB_DQ0
M_B_DQ1 A5 SB_DQ1
M_B_DQ2 C3 SB_DQ2
M_B_DQ3 B3 SB_DQ3
M_B_DQ4 E4 SB_DQ4
M_B_DQ5 A4 SB_DQ5
M_B_DQ6 A4 SB_DQ6
M_B_DQ7 C4 SB_DQ7
M_B_DQ8 D1 SB_DQ8
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M_B_DQ10 F2 SB_DQ10
M_B_DQ11 F1 SB_DQ11
M_B_DQ12 C2 SB_DQ12
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M_B_DQ15 G4 SB_DQ15
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M_B_DQ24 J5 SB_DQ24
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M_B_DQ50 AT4 SB_DQ50
M_B_DQ51 AN6 SB_DQ51
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M_B_DQ53 AN3 SB_DQ53
M_B_DQ54 AT5 SB_DQ54
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M_B_DQ56 AN7 SB_DQ56
M_B_DQ57 AP6 SB_DQ57
M_B_DQ58 AP8 SB_DQ58
M_B_DQ59 AT9 SB_DQ59
M_B_DQ60 AT7 SB_DQ60
M_B_DQ61 AP9 SB_DQ61
M_B_DQ62 AR10 SB_DQ62
M_B_DQ63 AT10 SB_DQ63

M_B_BS0 <<>> AB1 SB_BS0
M_B_BS1 <<>> W5 SB_BS1
M_B_BS2 <<>> R7 SB_BS2

M_B_CAS# <<>> AC5 SB_CAS#
M_B_RAS# <<>> Y7 SB_RAS#
M_B_WE# <<>> AC6 SB_WE#

CLARKSFIELD

DDR SYSTEM MEMORY - B

SB_CK0 W8 <<>> M_CLK_DDR2
SB_CK#0 W9 <<>> M_CLK_DDR#2
SB_CKE0 M3 <<>> M_CKE2

SB_CK1 V7 <<>> M_CLK_DDR3
SB_CK#1 V6 <<>> M_CLK_DDR#3
SB_CKE1 M2 <<>> M_CKE3

SB_CS#0 AB8 <<>> M_CS#2
SB_CS#1 AD6 <<>> M_CS#3

SB_ODT0 AC7 <<>> M_ODT2
SB_ODT1 AD1 <<>> M_ODT3

SB_DM0 D4 M_B_DM0
SB_DM1 E1 M_B_DM1
SB_DM2 H3 M_B_DM2
SB_DM3 K1 M_B_DM3
SB_DM4 AH1 M_B_DM4
SB_DM5 AL2 M_B_DM5
SB_DM6 AR4 M_B_DM6
SB_DM7 AT8 M_B_DM7

M_B_DM[7..0]

M_B_DQS#[7..0]

M_B_DQS[7..0]

M_B_A[15..0]

SB_DQS#0 D5 M_B_DQS#0
SB_DQS#1 F4 M_B_DQS#1
SB_DQS#2 J4 M_B_DQS#2
SB_DQS#3 L4 M_B_DQS#3
SB_DQS#4 AH2 M_B_DQS#4
SB_DQS#5 AL4 M_B_DQS#5
SB_DQS#6 AR5 M_B_DQS#6
SB_DQS#7 AR8 M_B_DQS#7

SB_DQS0 C5 M_B_DQS0
SB_DQS1 E3 M_B_DQS1
SB_DQS2 H4 M_B_DQS2
SB_DQS3 M5 M_B_DQS3
SB_DQS4 AC2 M_B_DQS4
SB_DQS5 AL5 M_B_DQS5
SB_DQS6 AP5 M_B_DQS6
SB_DQS7 AR7 M_B_DQS7

SB_MA0 U5 M_B_A0
SB_MA1 V2 M_B_A1
SB_MA2 T5 M_B_A2
SB_MA3 V3 M_B_A3
SB_MA4 R1 M_B_A4
SB_MA5 T8 M_B_A5
SB_MA6 R2 M_B_A6
SB_MA7 R6 M_B_A7
SB_MA8 R4 M_B_A8
SB_MA9 R5 M_B_A9
SB_MA10 AB5 M_B_A10
SB_MA11 P3 M_B_A11
SB_MA12 R3 M_B_A12
SB_MA13 AE7 M_B_A13
SB_MA14 P5 M_B_A14
SB_MA15 N1 M_B_A15

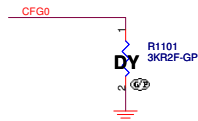
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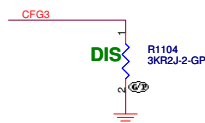
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Size: Document Number: **Berry** Rev: **X00**

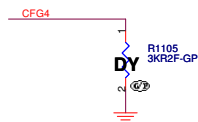
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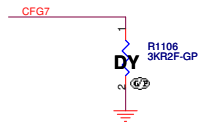
PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled



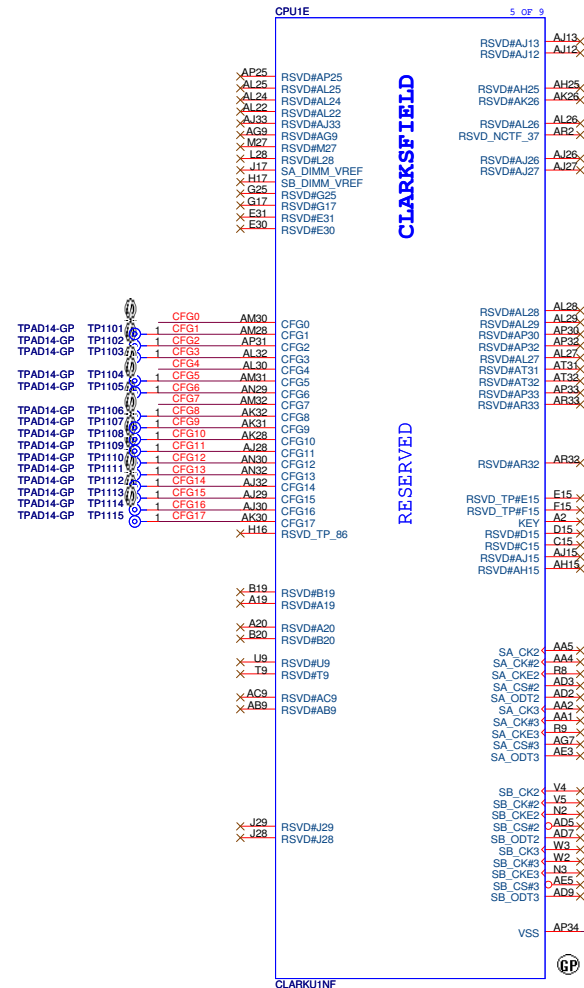
CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 : Normal Operation 0 : Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



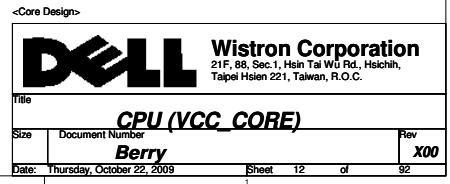
CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

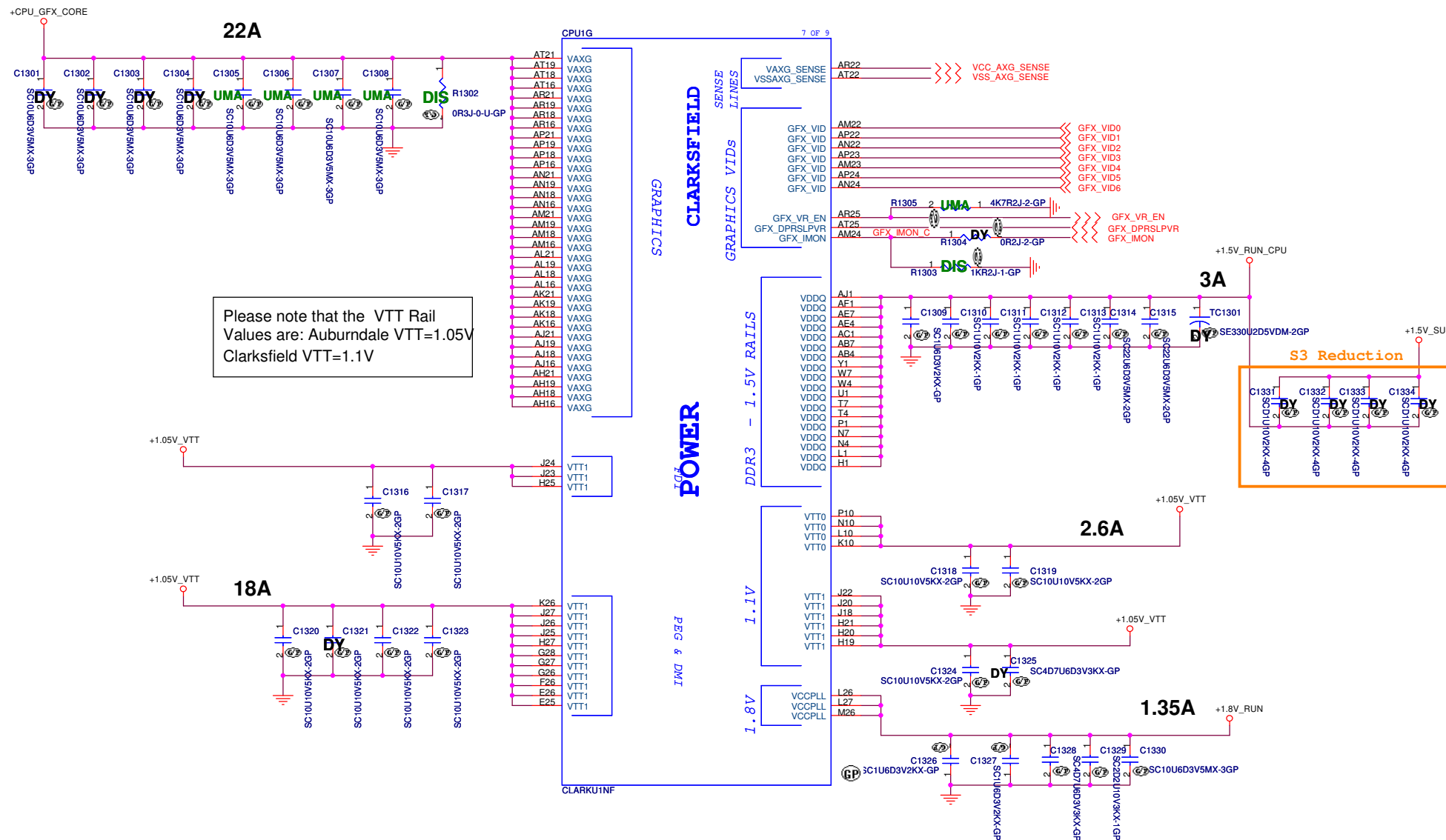


CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	<p>Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor.</p> <p>Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.</p>



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND.



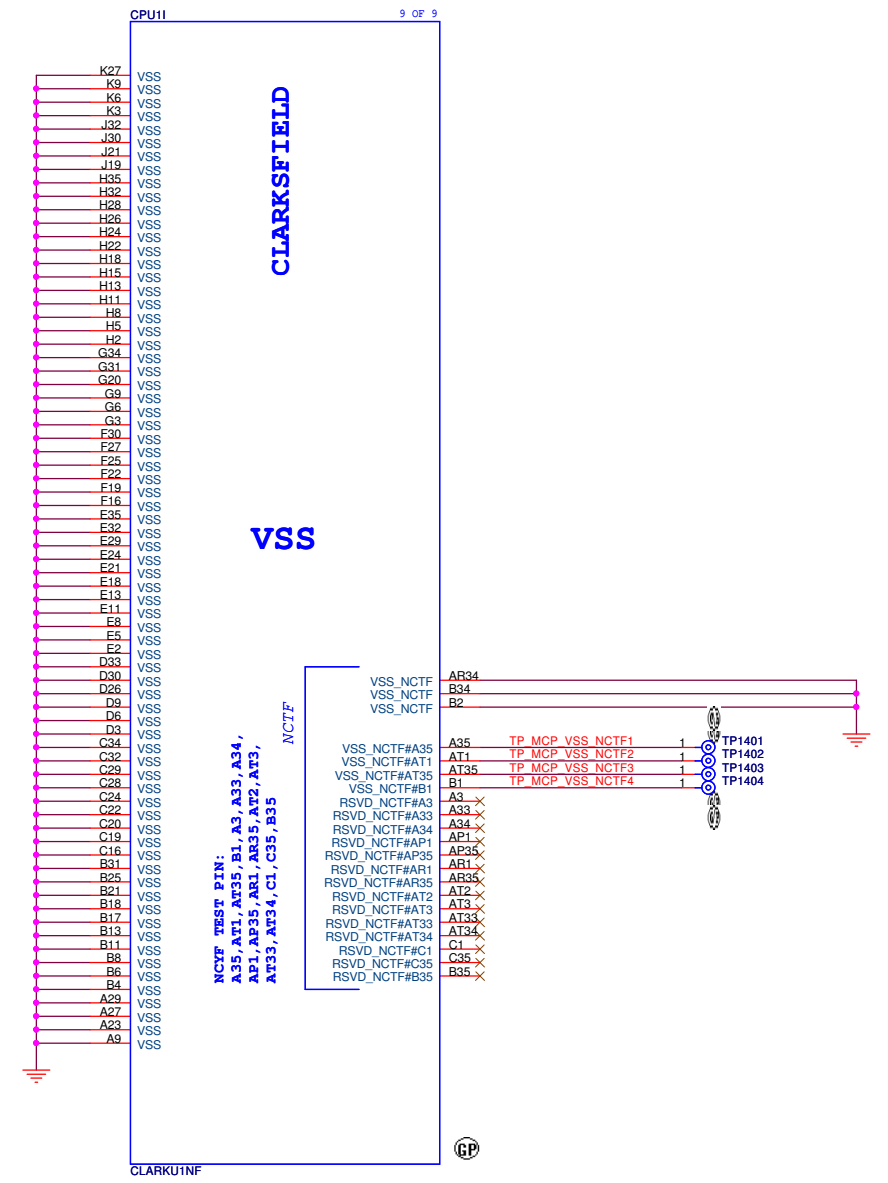
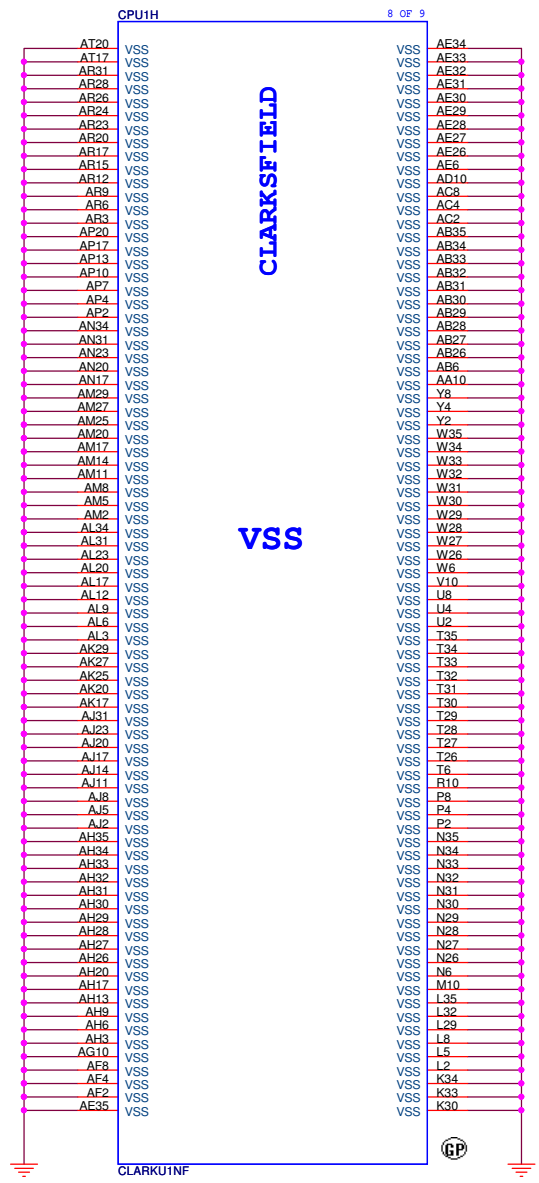


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Date:

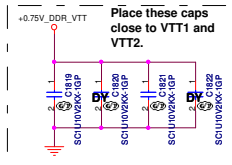
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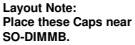
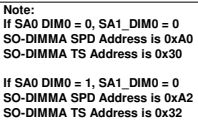
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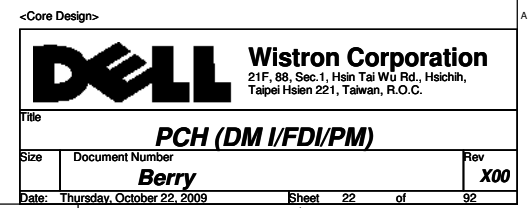
SEC. 62.10017.P11



SO-DIMMB is placed farther from the Processor than SO-DIMMA









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Title **PCH (SPI/RTC/LPC/SATA/IHDA)**

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Size	Document Number
	Bernie

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Rev	X00
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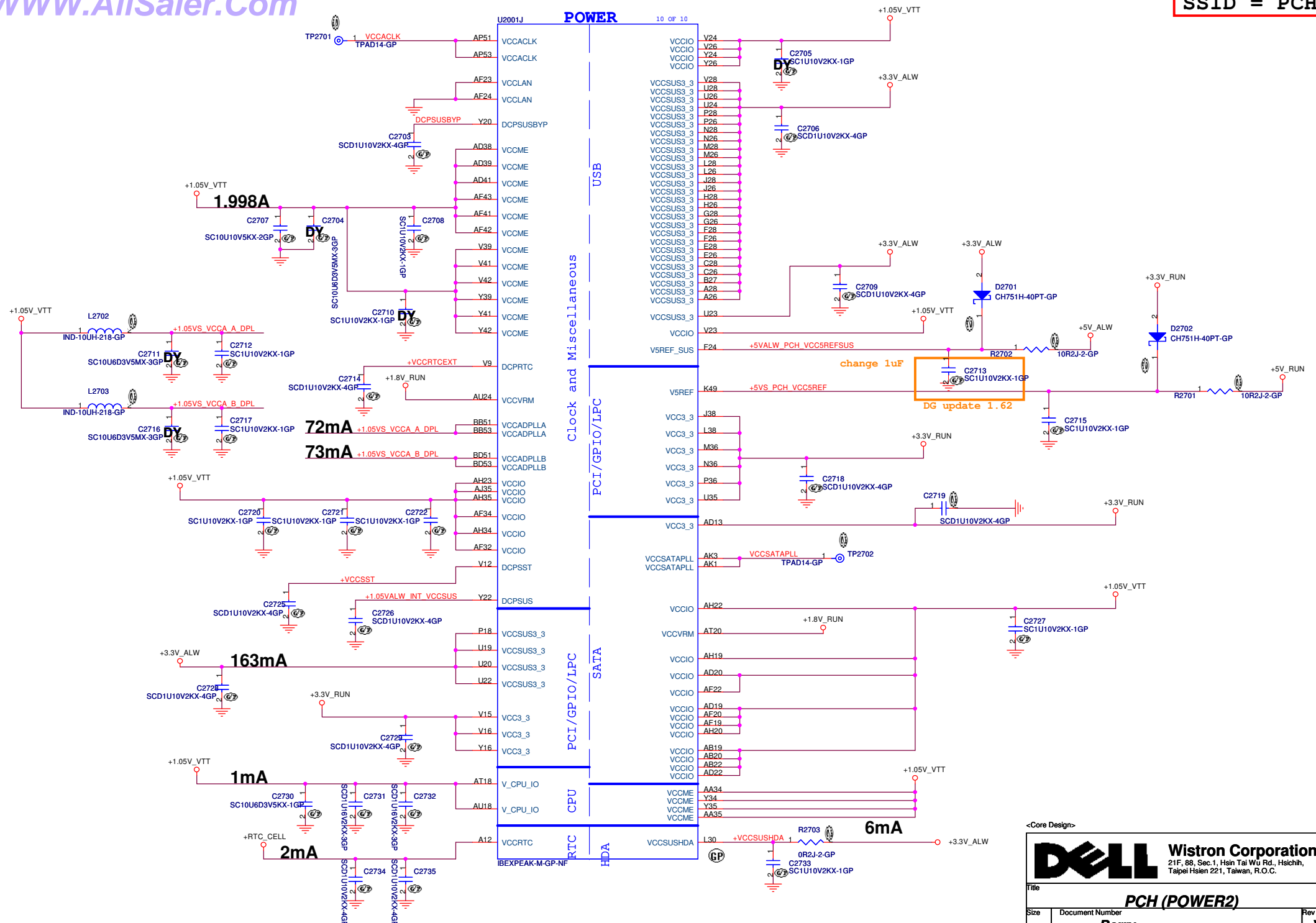
PCH (GPIO/CPU)

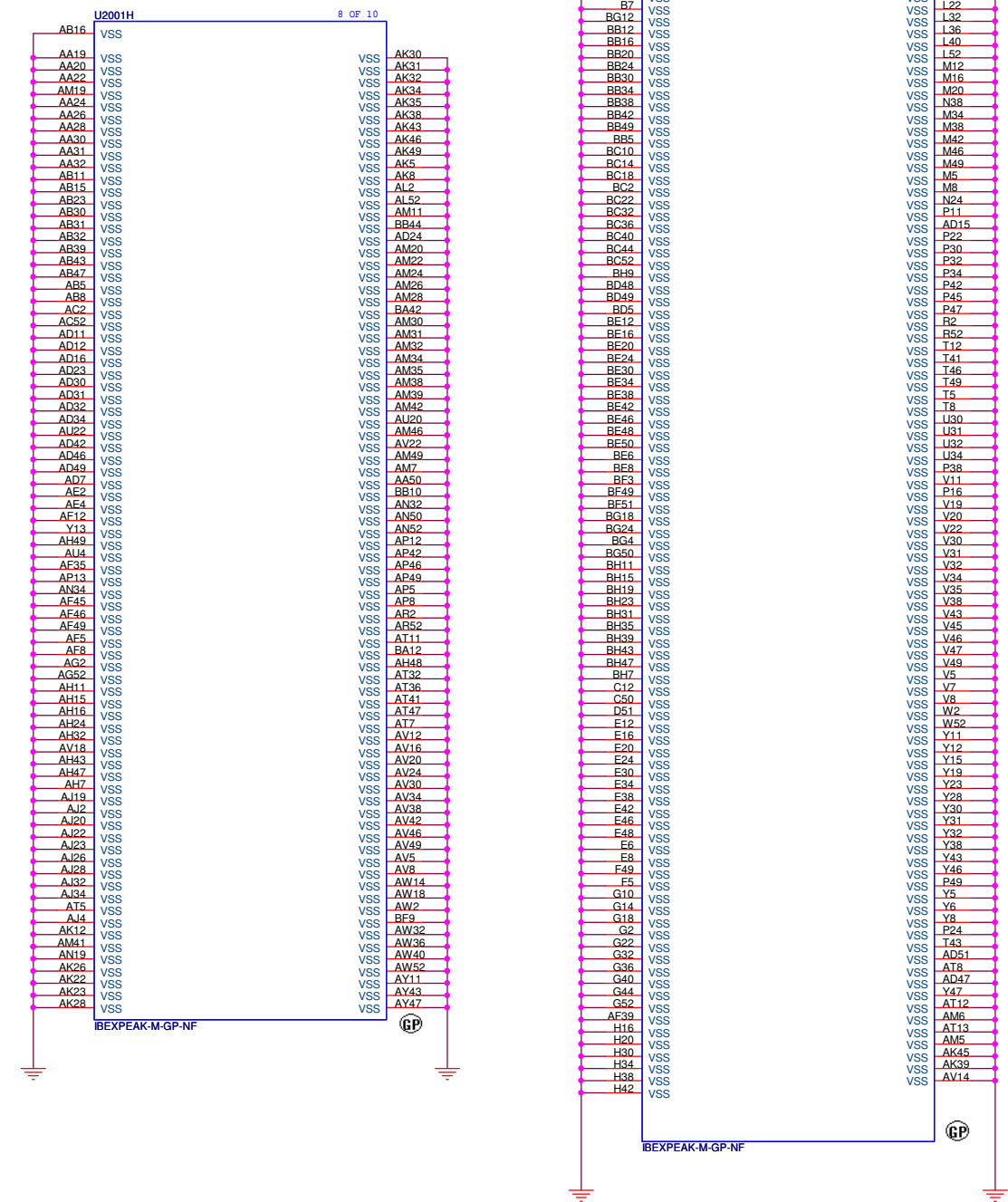
Rev

X00

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<Core Design>

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.


Title: **PCH (VSS)**

Size: Document Number: **Berry** Rev: **X00**

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<Core Design>



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Title

Reserved

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AUD_CAP2

AUD_VREFFLT

AUD_V B

AUD_VREG

C3017

20k

100n

SC10160AUD_XM5V6X50P

AUD_AGN2

C3018

20k

100n

SC10160AUD_XM5V6X50P

AUD_AGN2

C3019

20k

100n

SC10160AUD_XM5V6X50P

AUD_AGN2

C3016

20k

100n

SC10160AUD_XM5V6X50P

AUD_AGN2


Close to codec

PCH_SDOUT_CODEC

Close to Pin14

(Blanking)

<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size
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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title


Reserved

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title


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<Core Design>



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Title

Size

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Berry

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Wednesday, October 14, 2009

Rev

X00

Sheet


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92

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<Core Design>



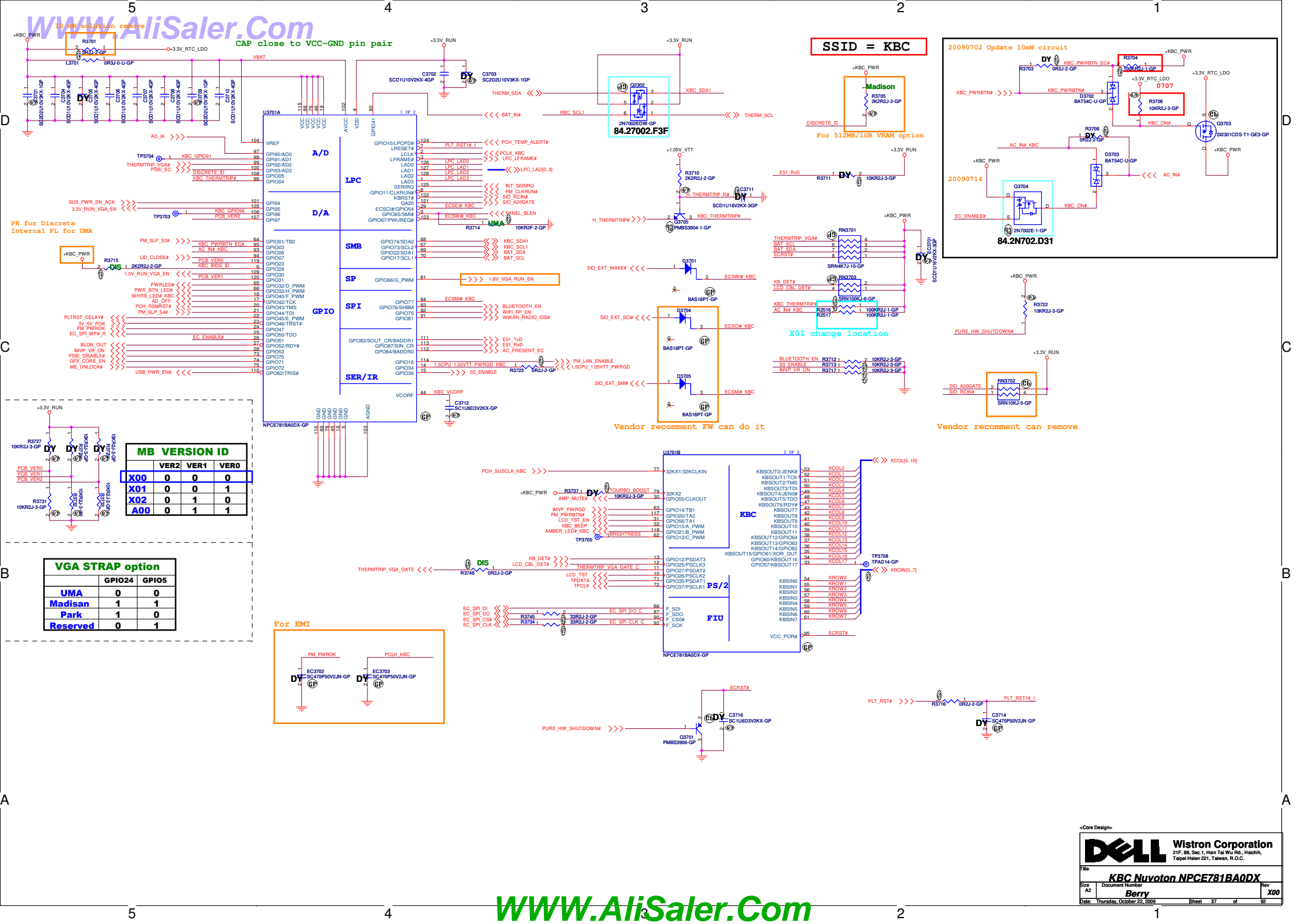
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size	Document Number	Rev
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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A4

Document Number

Berry

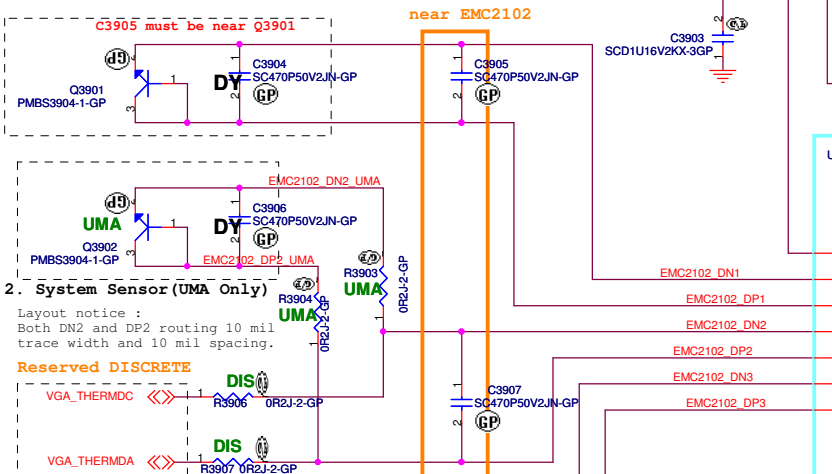
Rev
X00

Date: Wednesday, October 14, 2009

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1. Place near CPU PWM CORE and PCH.

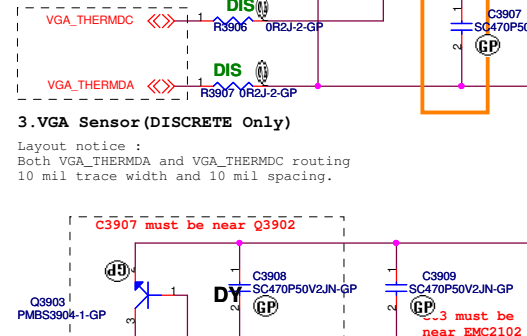
Layout notice :
Both DN1 and DP1 routing 10 mil
trace width and 10 mil spacing.



2. System Sensor (UMA Only)

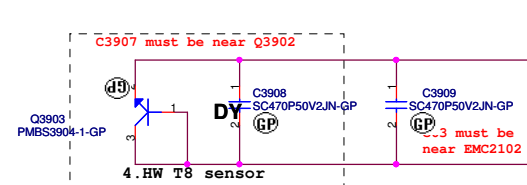
Layout notice :
Both DN2 and DP2 routing 10 mil
trace width and 10 mil spacing

Reserved DISCRETE

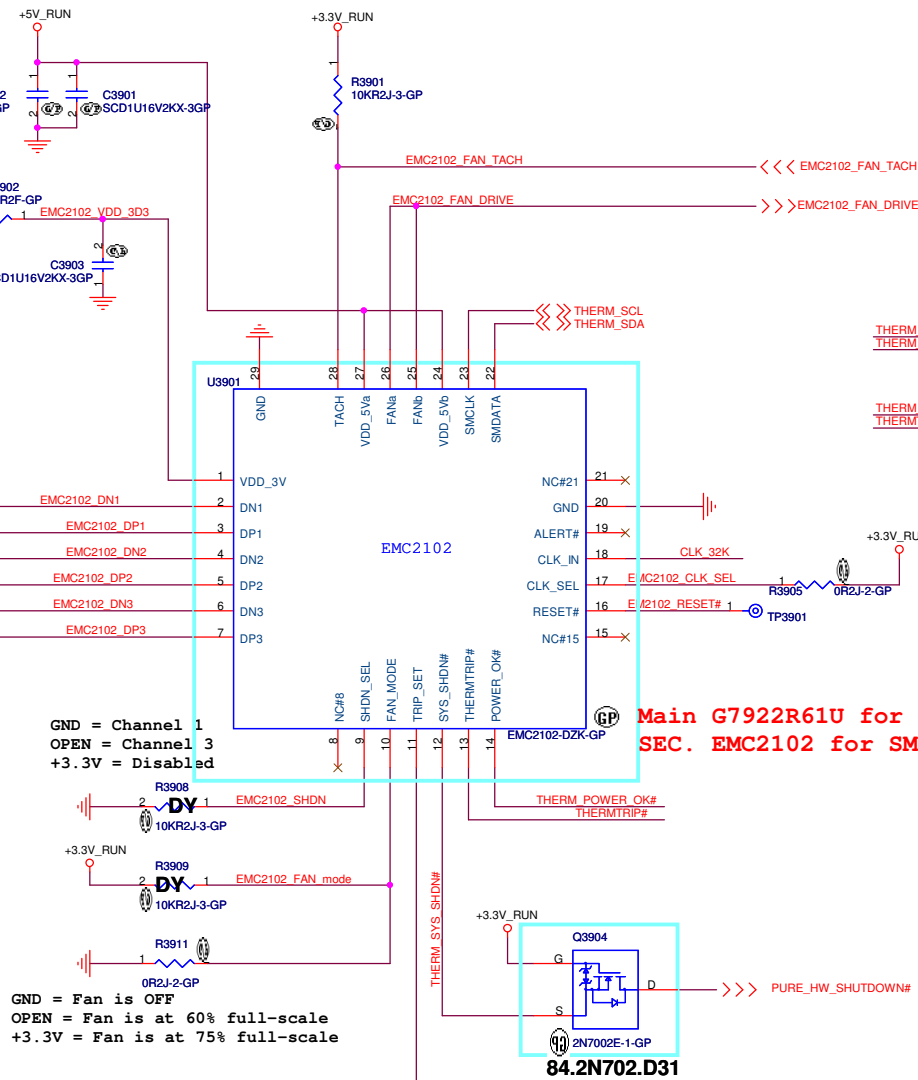


3.VGA Sensor (DISCRETE Only)

Layout notice :
Both VGA_THERMDA and VGA_THERMDC routing
10 mil trace width and 10 mil spacing.

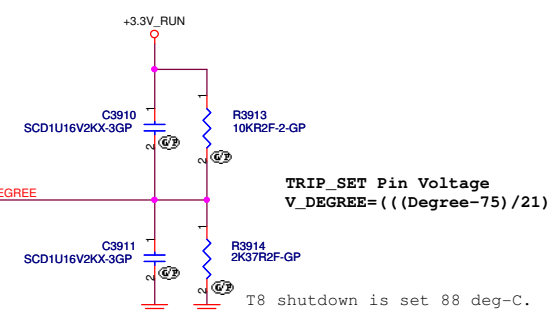
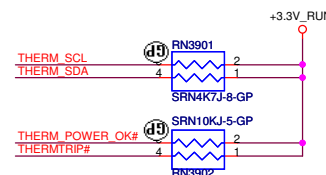


Layout notice :
Both DN3 and DP3 routing 10 mil
trace width and 10 mil spacing.



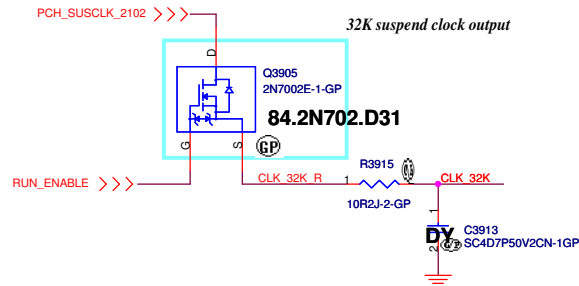
Main G7922R61U for GMT P/N:74.07922.0B3
SEC. EMC2102 for SMSC P/N:74.02102.A73

```
GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected
```



TRIP_SET Pin Voltage
V DEGREE=((Degree-75)/21)

T8 shutdown is set 88 deg-C.



32K suspend clock output

84.2N702.D31

Core Design




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Title			
Thermal/Fan Controllor EMC2102			
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Custom	Berry		X0
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<Core Design>



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Title


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<Core Design>



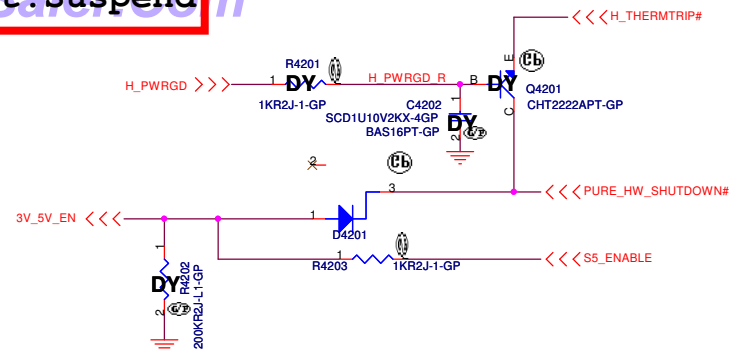
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

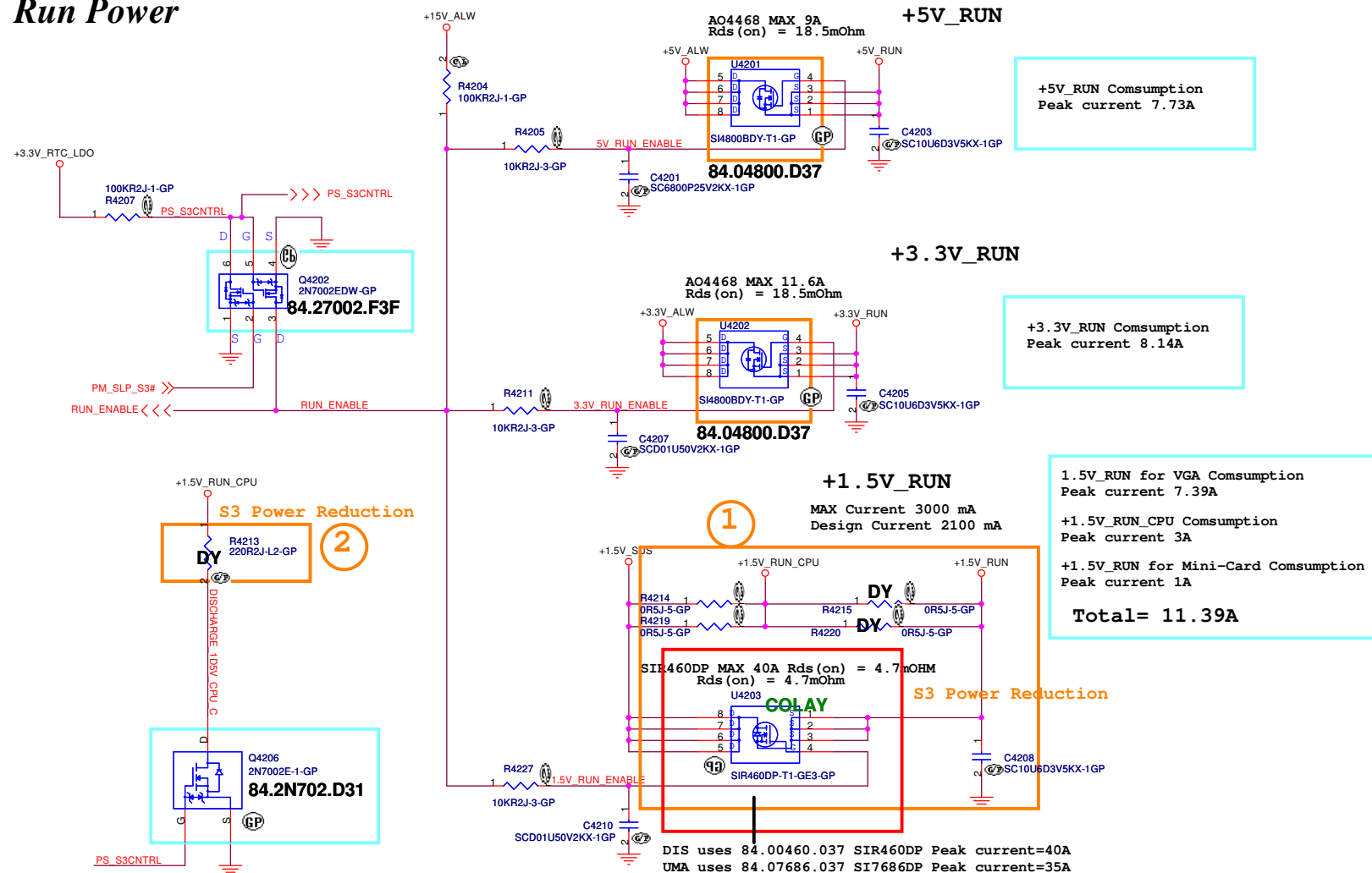
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Run Power



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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size

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Document Number

Berry

Date:

Wednesday, October 14, 2009

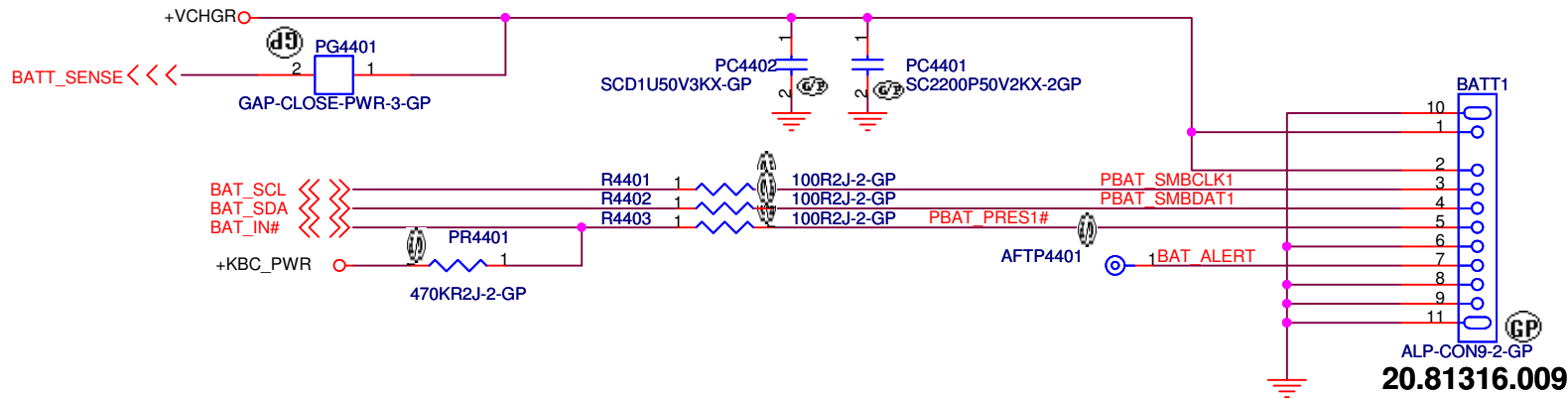
Rev

X00

Reserved

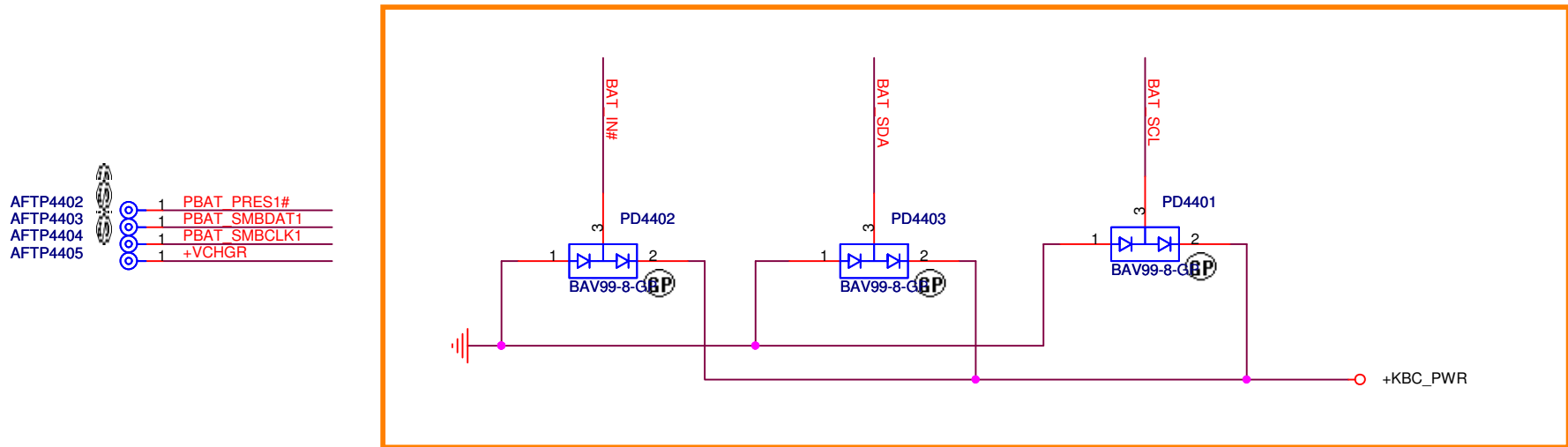
Sheet 43 of 92

Batt Connector



For actual location, need to be swap all pin

Close to Batt Connector



<Core Design>



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Title

BATT CONN

Size
A4

Document Number

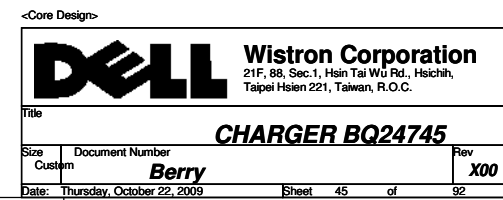
Berry

Rev

X00

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Design Current = 9.07A
14.25A < OCP < 16.84A

Design Current = 8.48A
13.32A < OCP < 15.75A

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3UH PCMB104T-3R3MS Cyntec 10.8mohm/11.8mohm Isat =16Arms 68.3R310.20C
O/P cap: 220U 6.3V PSLV0J227M(25) 25mohm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V TEPSLB20J107M(45) 8R 45mohm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: FDS8880 9.6mohm/12mohm@4.5Vgs/ 84.08880.037
L/S: FDS6676AS 5.9mohm/7.25mohm@4.5Vgs/ 84.06676.A37


TPS51125:		CH1	CH2	SKIPSEL	VREG3 or VREG5	VREF(2V)	GND
TONSEL		200kHz	265kHz	Operating Mode	OOA Auto Skip	Auto Skip	PWM only
VREF		245kHz	305kHz				
VREG3		300kHz	375kHz				
VREG5		365kHz	460kHz				

EN0	Operating Mode	820k to GND	GND
Open	enable both IDOs, VCLK on and ready to turn on switcher channels	enable both IDOs, VCLK off and ready to turn on switcher channels	disable all circuit

RT8205B:		
TONSEL	CH1	CH2
GND	200kHz	250kHz
VREF	300kHz	375kHz
VREG3	365kHz	460kHz
VREG5	365kHz	460kHz

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<Core Design>



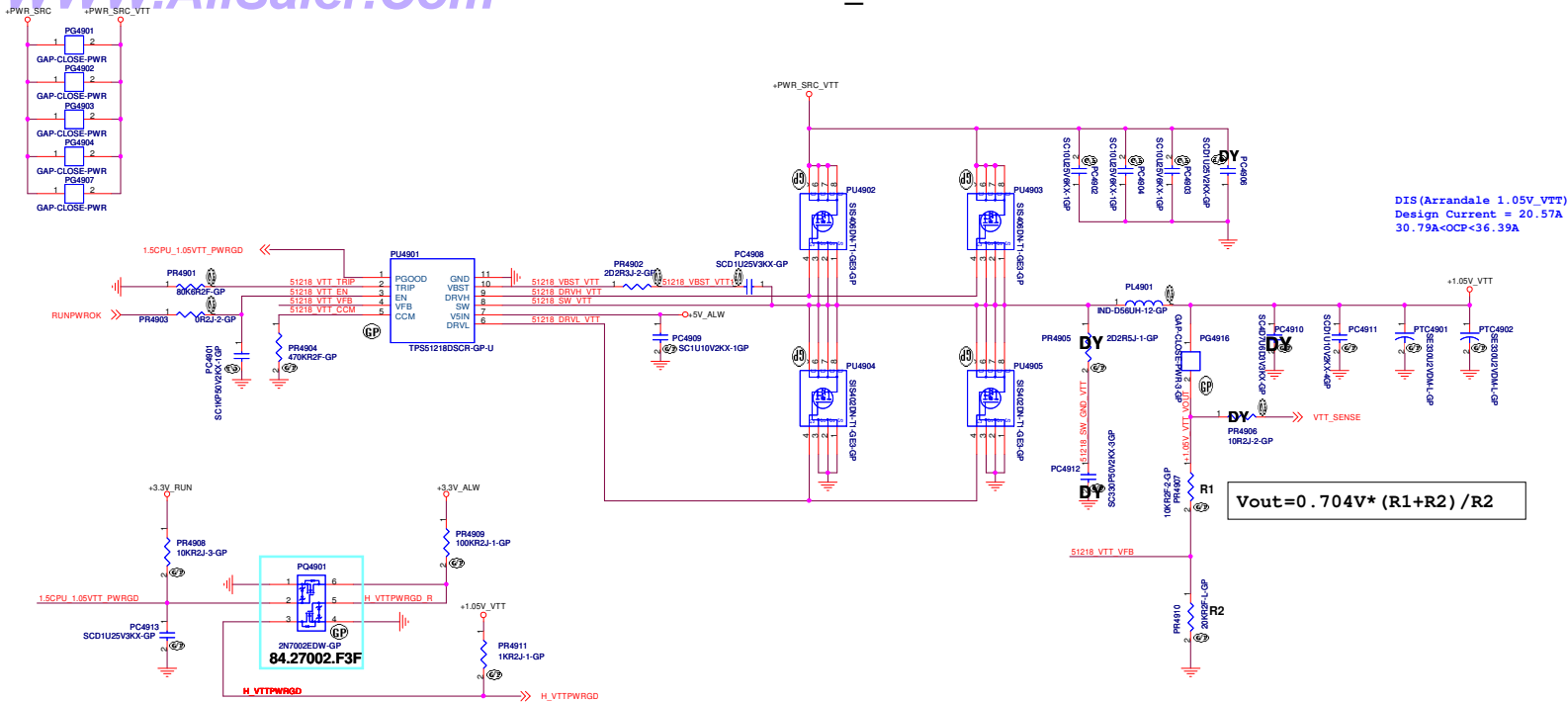
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size A3	Document Number Berry	Rev X00
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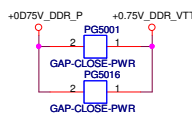
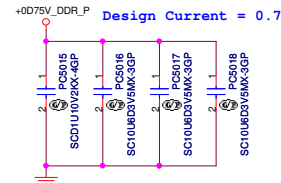
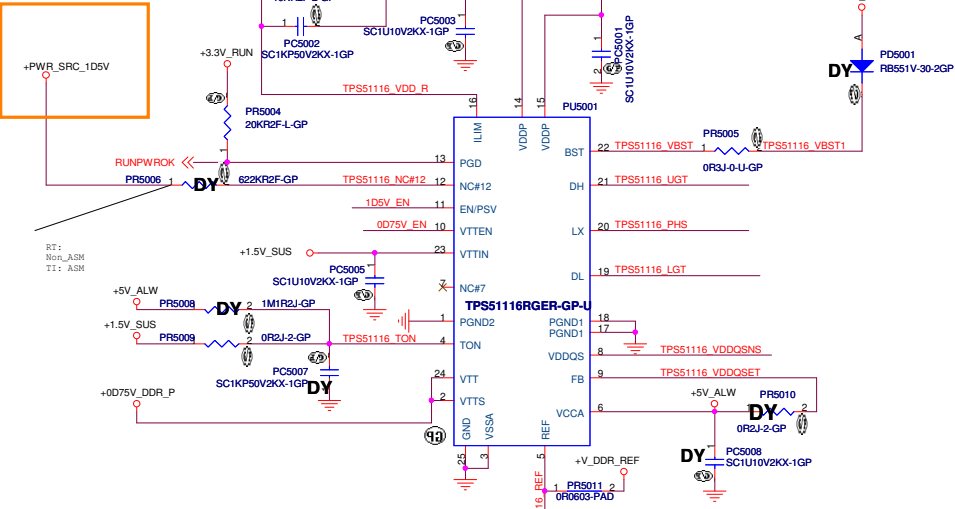
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Frequency setting	
470K	-->290KHz
200K	-->340KHz
100K	-->380KHz
39K	-->430KHz

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cynotec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEF5X0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: SIS406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm 84.5Vgs/ 84.00406.037
L/S: SIS402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037

Modified net name

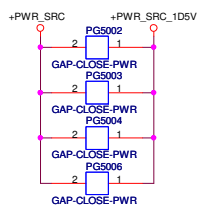
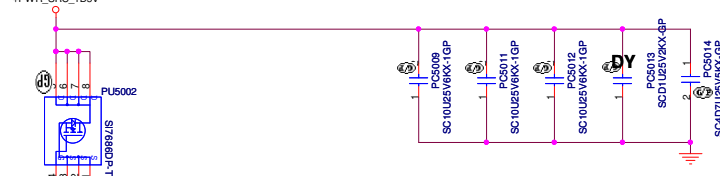
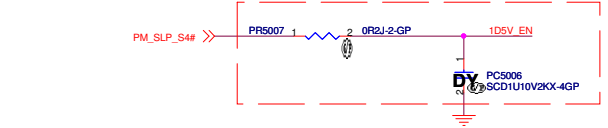
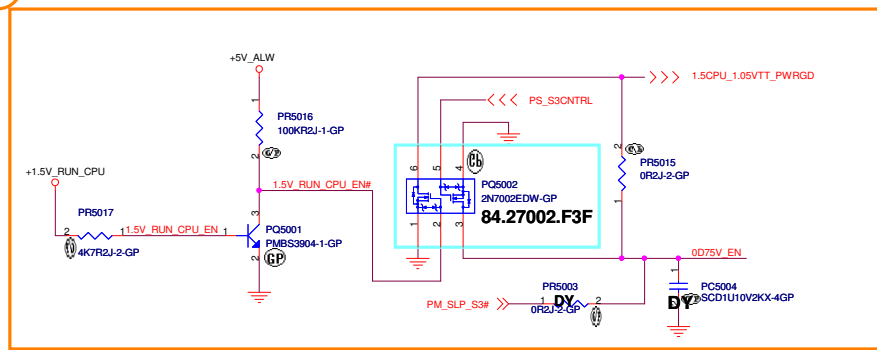


State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

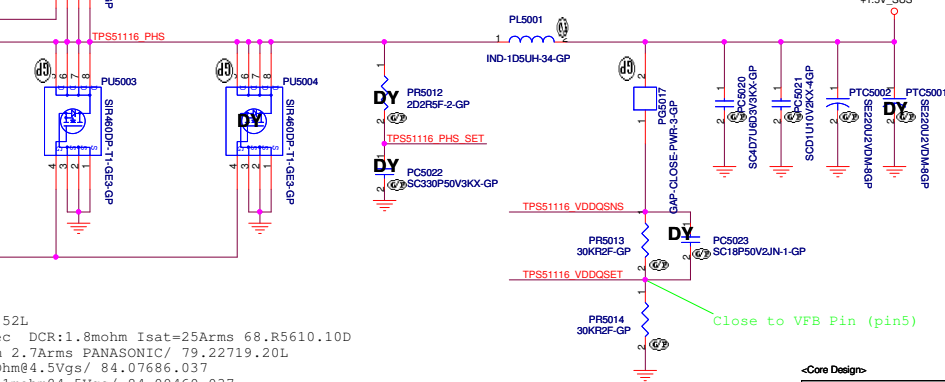
VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 220U 2V EEFCXD221ER 15mOhm 2.7Arms PANASONIC/ 79.22719.20L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037
Switching freq->400KHz

5 S3 Power Reduction



Design Current = 14.45A
22.71A < OCP < 26.84A



Close to VFB Pin (pin5)

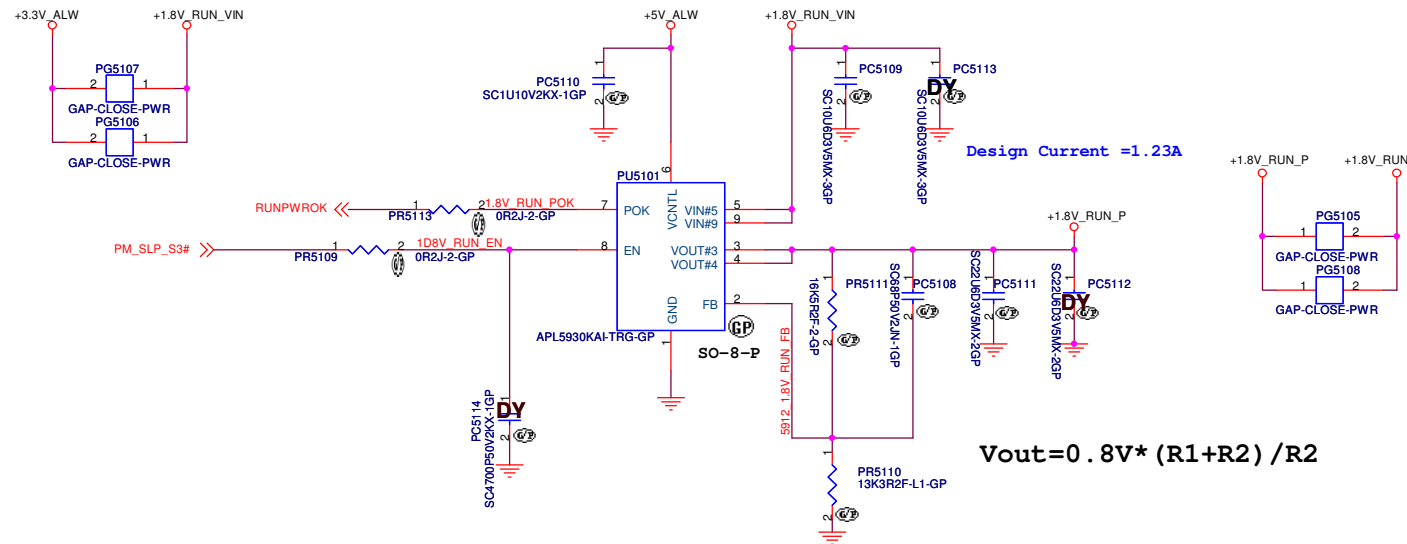
Wistron Corporation
21F, 8B, Sec.1, Hsin Tai Wu Rd., Hsichang, Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51116 +1.5V SUS**

Size: Custom
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APL5930 for +1.8V_RUN



$$V_{out} = 0.8V * (R1 + R2) / R2$$

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size

A3

Document Number

Berry

Date:

Wednesday, October 14, 2009

Rev

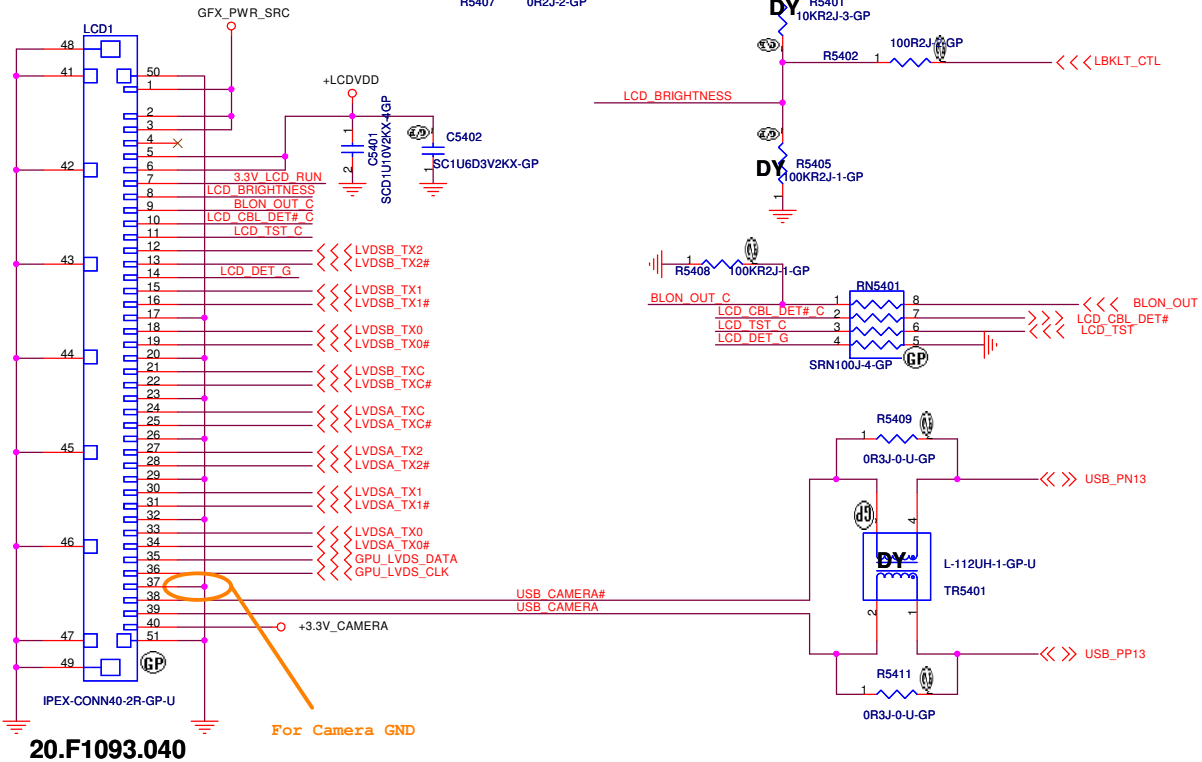
X00

Reserved

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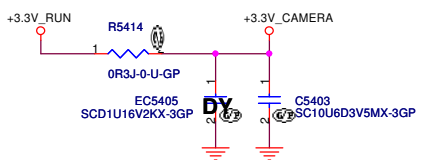
LVDS CONNECTOR



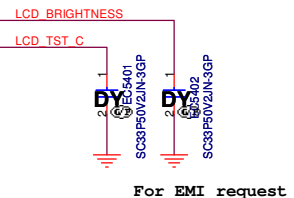
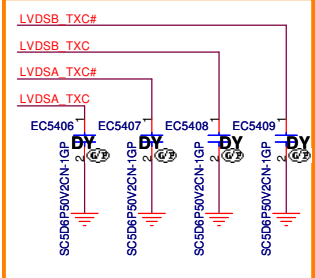
20.F1093.040

For Camera GND

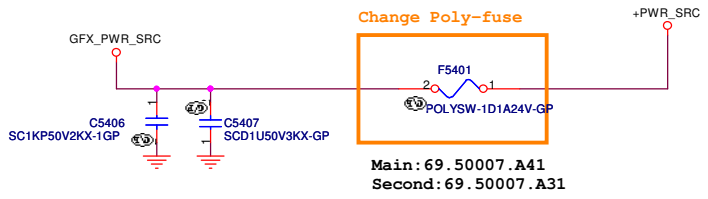
Camera Power



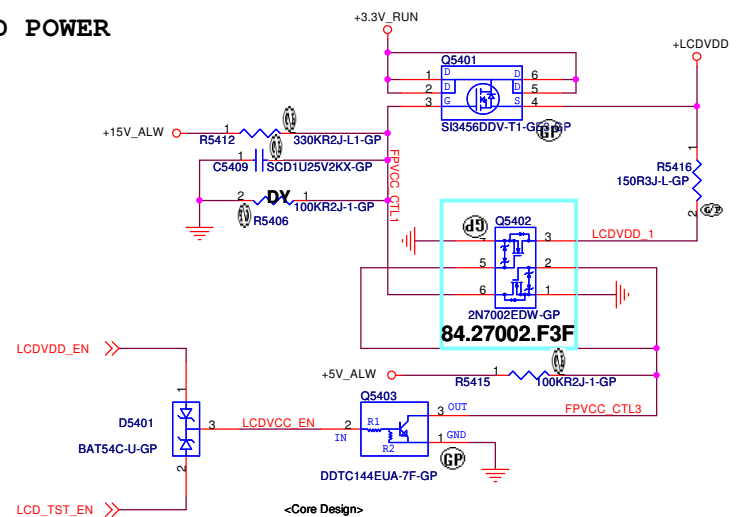
Close to LVDS connector



INVERTER POWER



LCD POWER



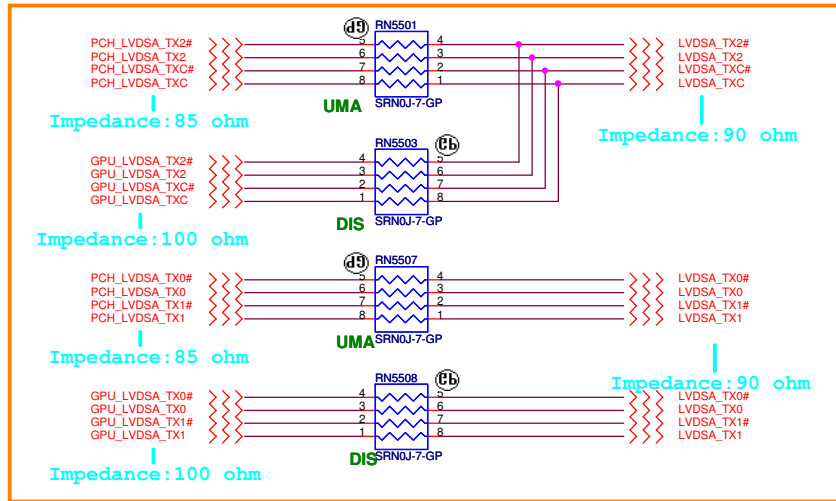
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD/Inverter Connector**

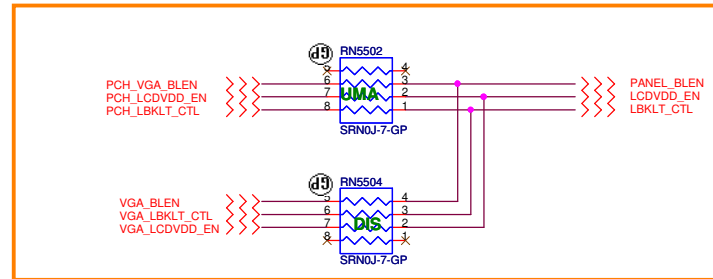
Size: A3 Document Number: **Berry** Rev: **X00**

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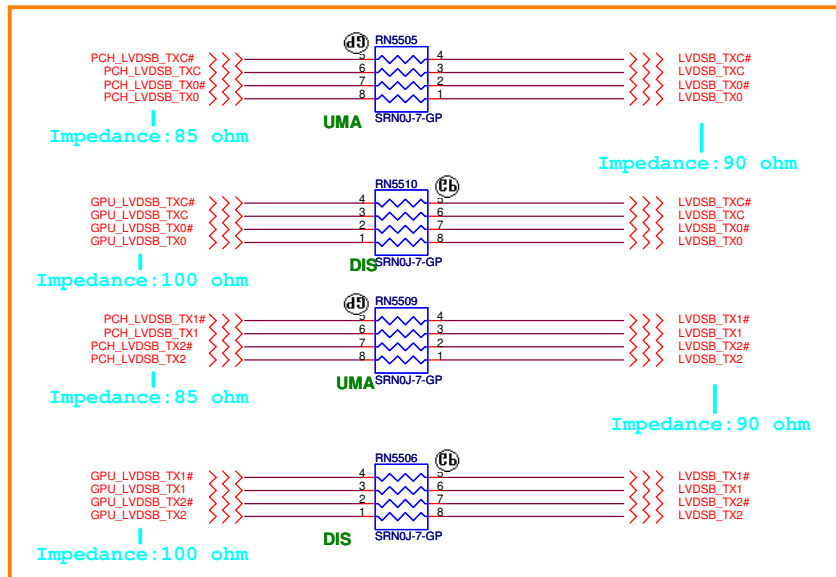
LVDS Channel A



Panel BL brightness/Power En/BL En



LVDS Channel B




<Core Design>

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LVDS Switch			
Size	Document Number	Rev	
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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

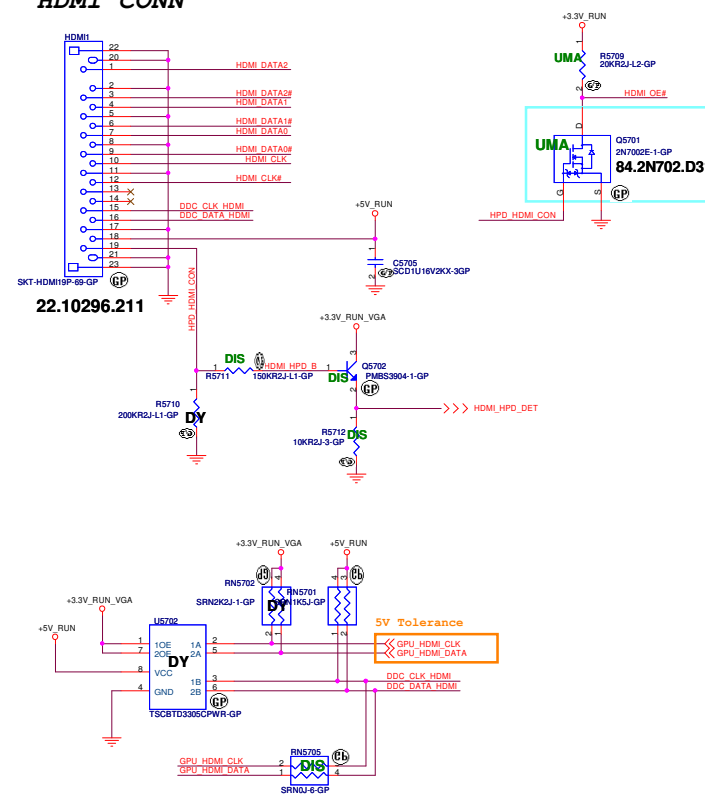
Title

LVDS Switch

Size A3	Document Number Berry	Rev X00
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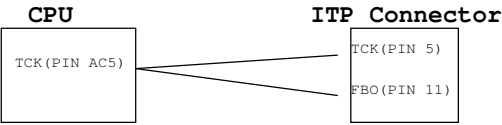
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HDMI Level Shifter & CONNECTOR



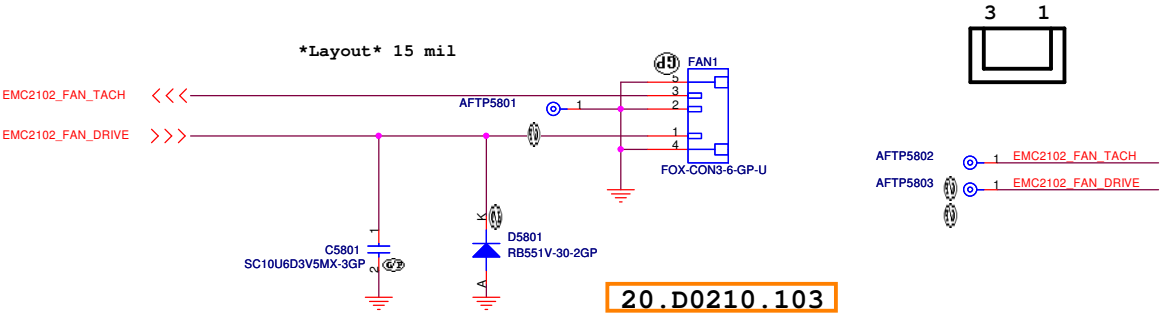
ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.

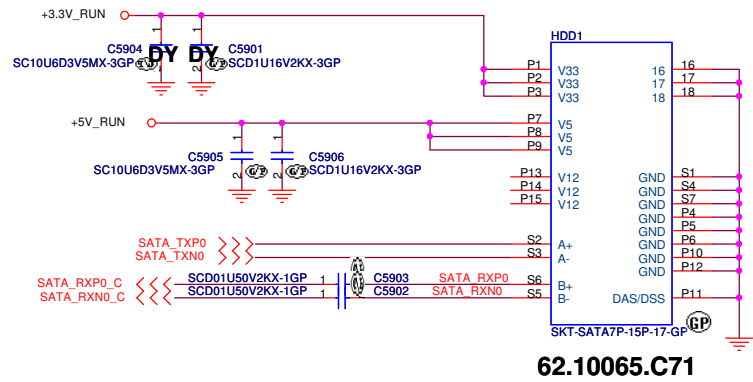


SSID = Thermal

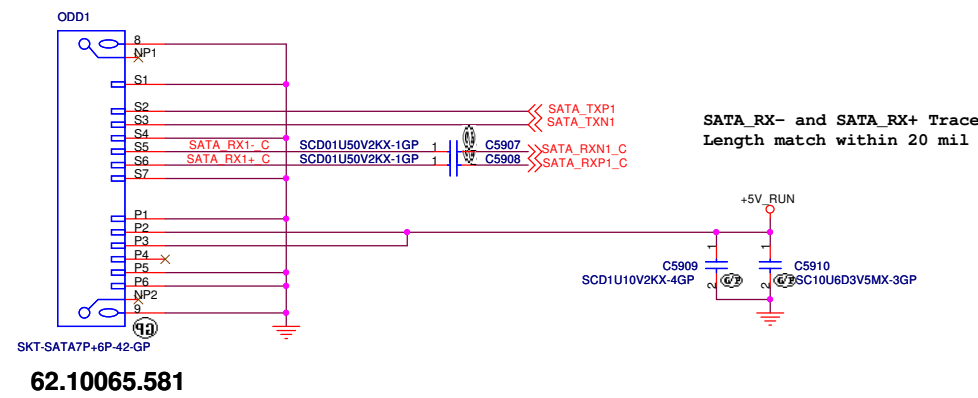
Fan Connector



SATA HDD Connector

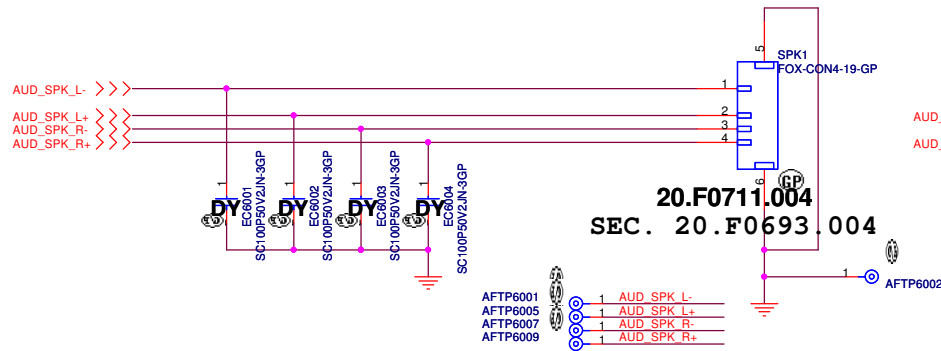


ODD Connector

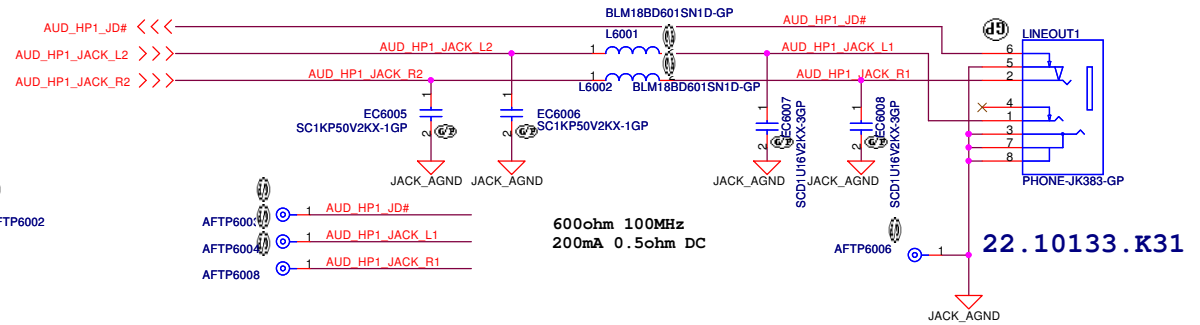


SSID = AUDIO

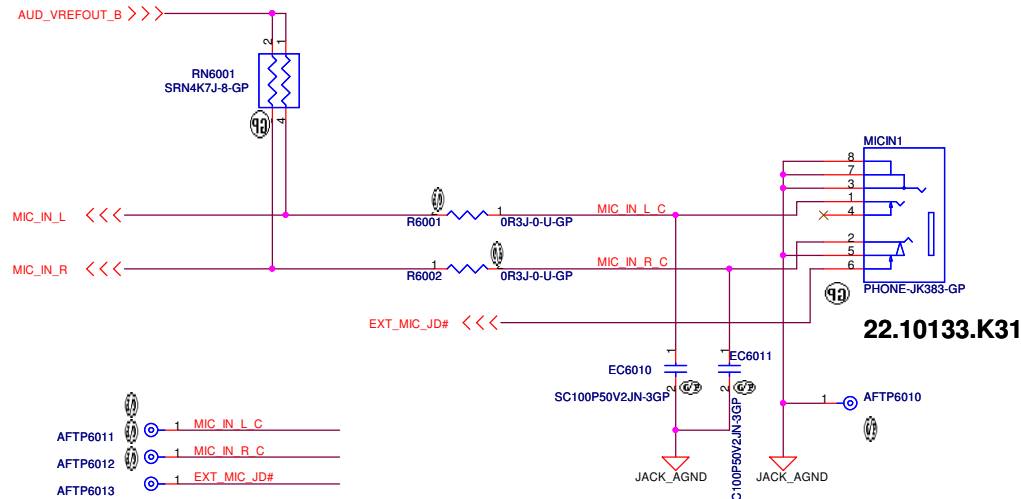
Speaker Connector



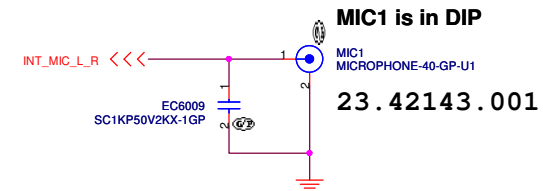
LINE1 OUT



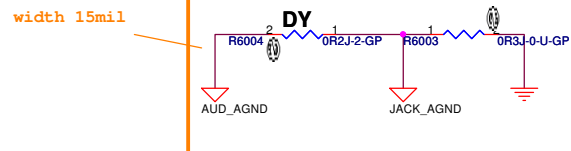
MIC IN



Internal Microphone



Close Jack




<Core Design>

DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		Audio Jack	
Size A3	Document Number	Rev X00	
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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

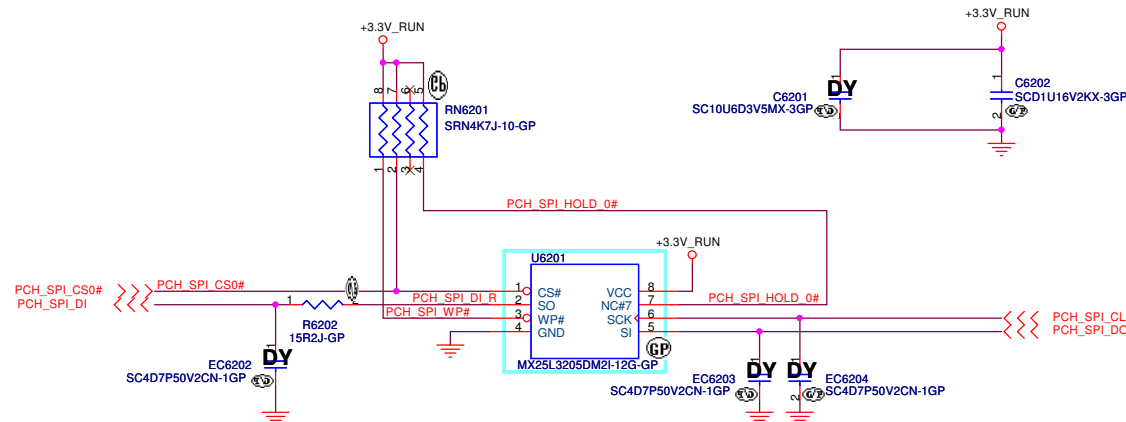
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Size	Document Number	Rev
A3	Berry	X00

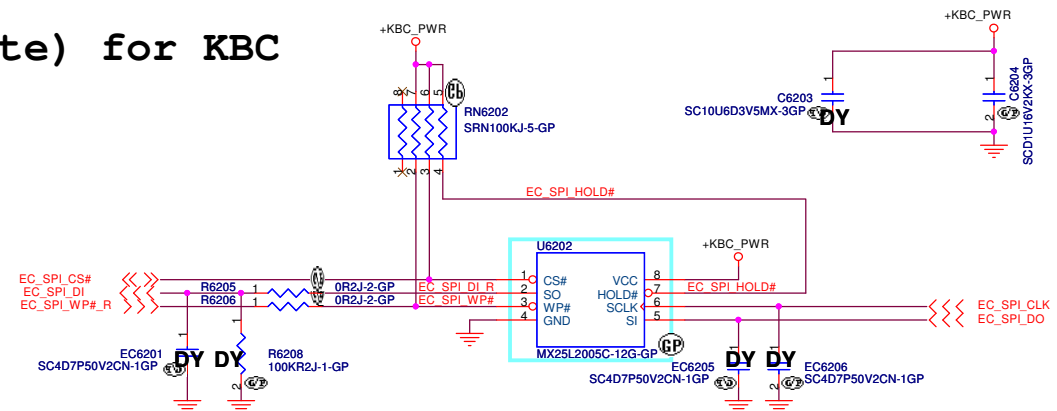
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Com

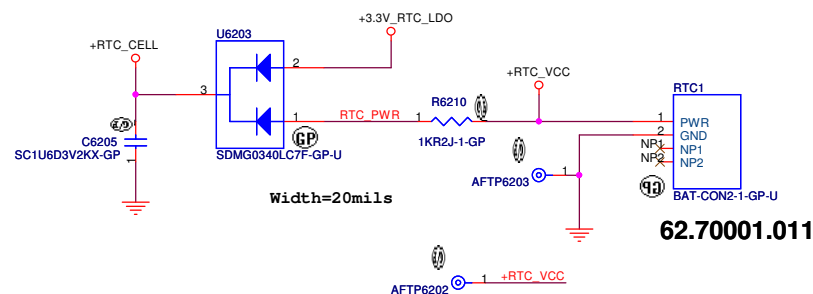
SPI FLASH ROM (4M byte) for PCH



SPI FLASH ROM (256K byte) for KBC



SSID = RBATT



<Core Design>



Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Flash/RTC

Size
A3

Document Number	Boon
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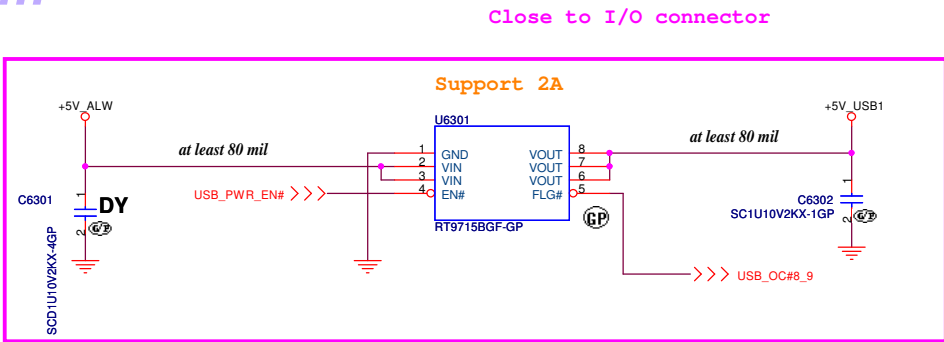
Date: Thursday, October 22, 2009

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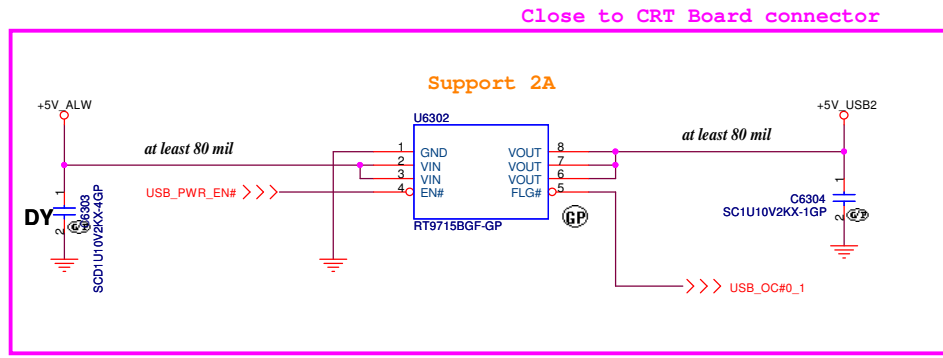
WWW.AliSaler.Com

IO Board USB Power

Main RT9715BGF P/N:74.09715.B79
SEC G547F2P81U P/N: 74.00547.A79



CRT Board USB Power



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Title

Reserved

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<Core Design>



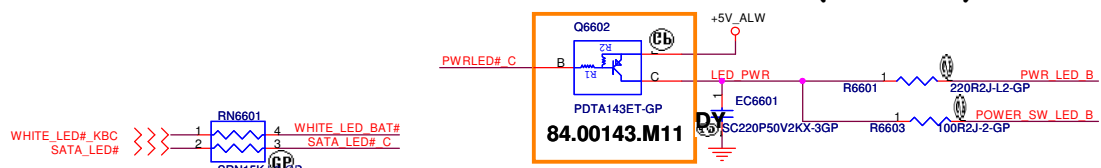
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

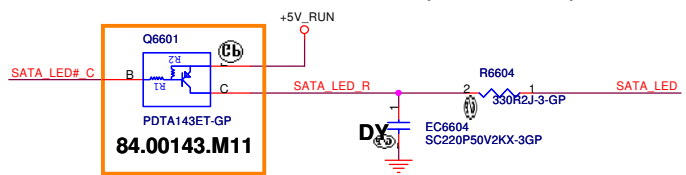
Reserved

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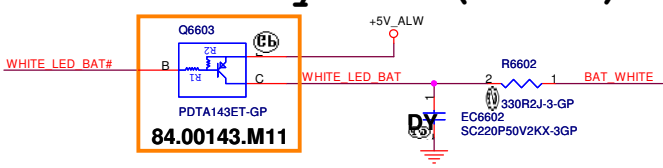
Power LED (White)



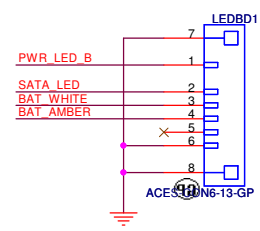
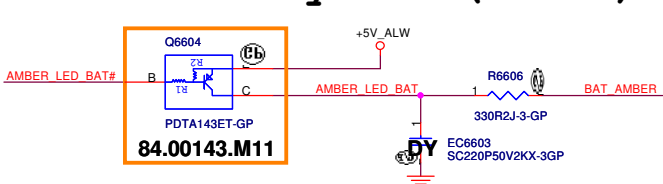
SATA HDD LED (White)



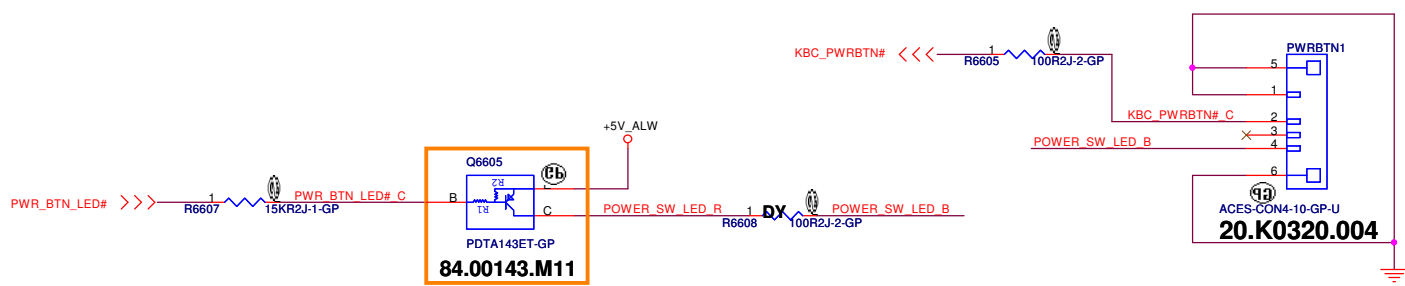
Battery LED1 (White)



Battery LED2 (Amber)




Power button LED (White)



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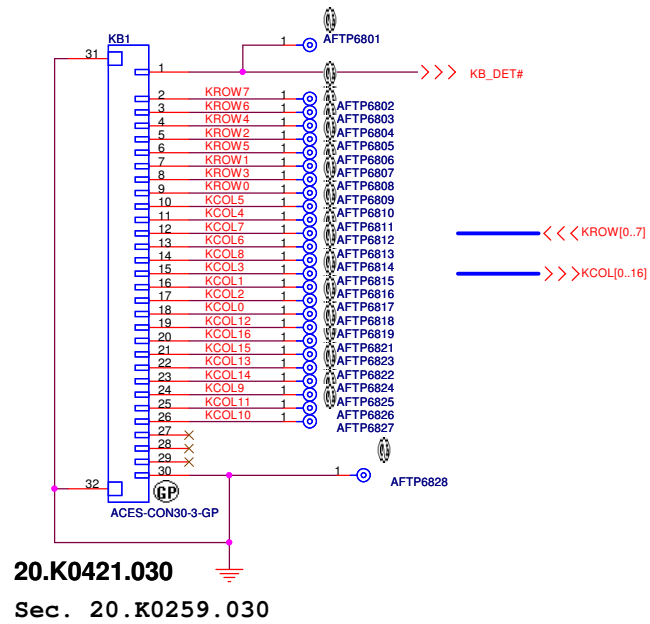
Document Number
Berry

Date: Wednesday, October 14, 2009

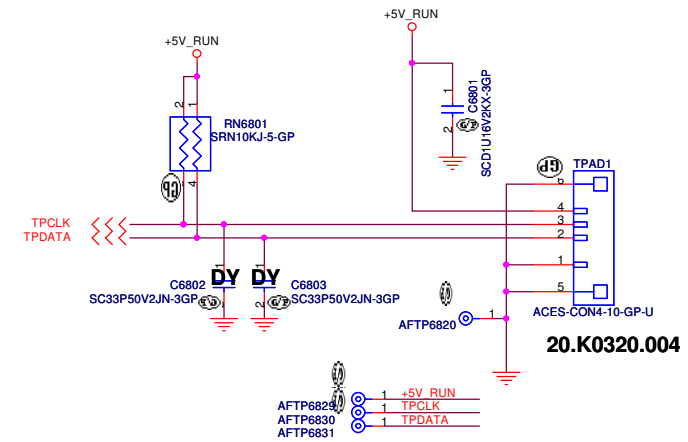
Rev
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Internal KeyBoard Connector



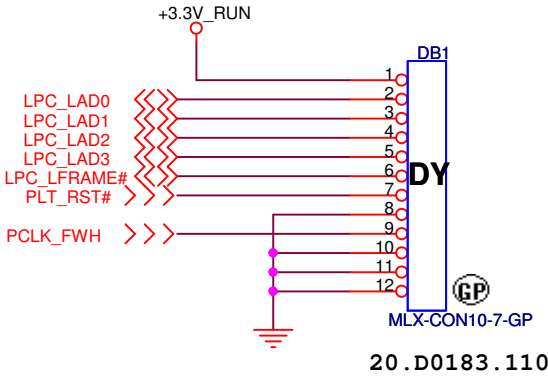
TouchPad Connector




<Core Design>



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<Core Design>

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Dubug connector			
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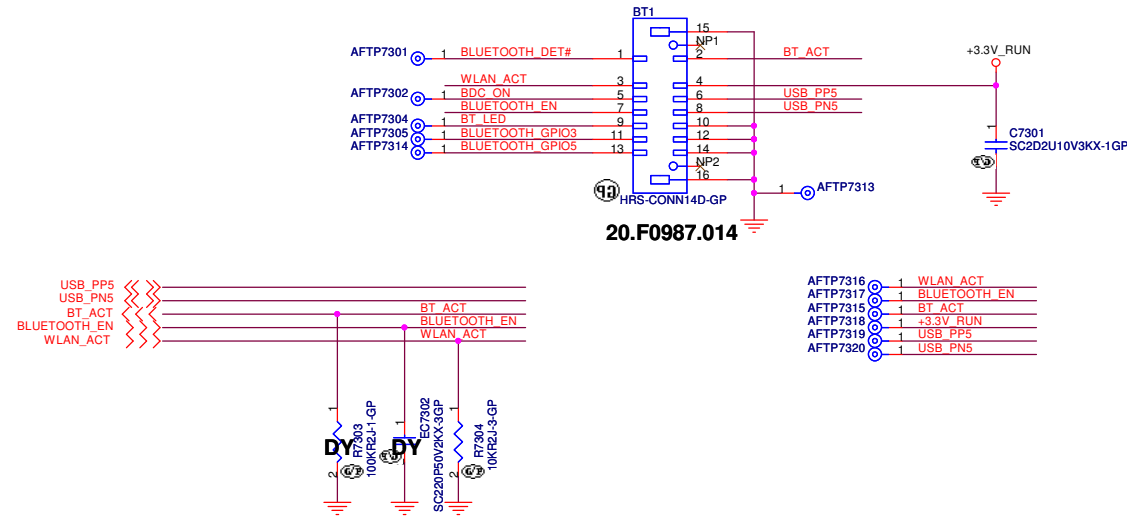
Title

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SSID = User.Interface

Bluetooth Module conn.



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Bluetooth

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Berry

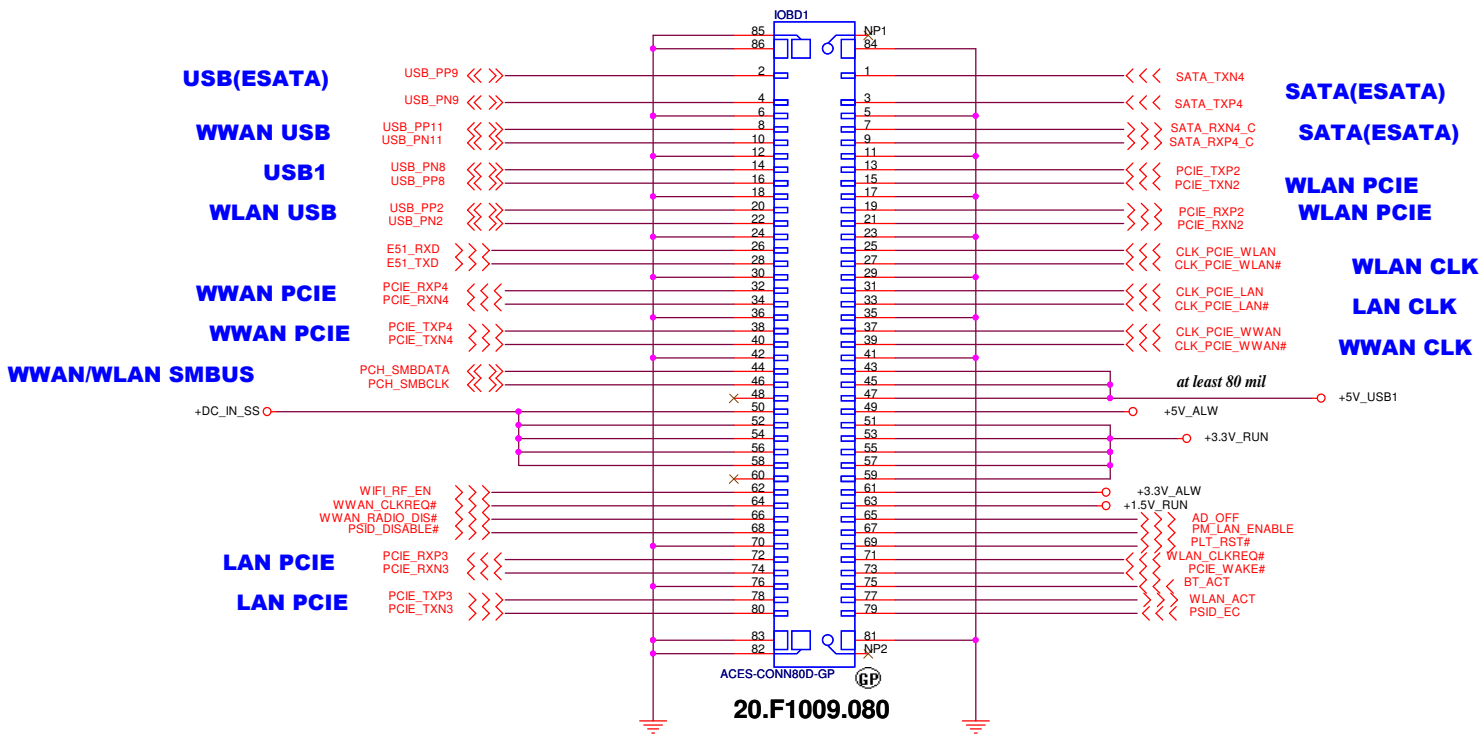
Rev

X00

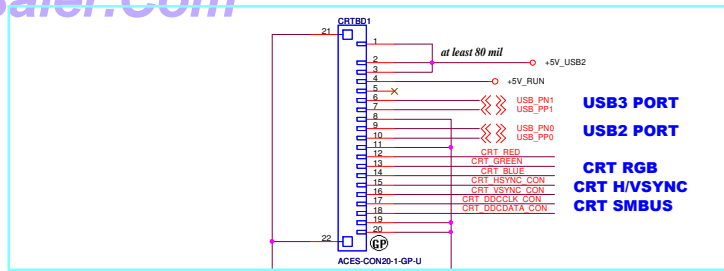
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IO Board CONN 80 pin

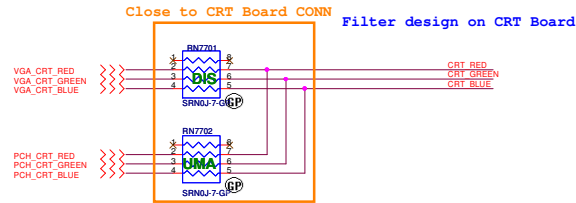


CRT Board Connector

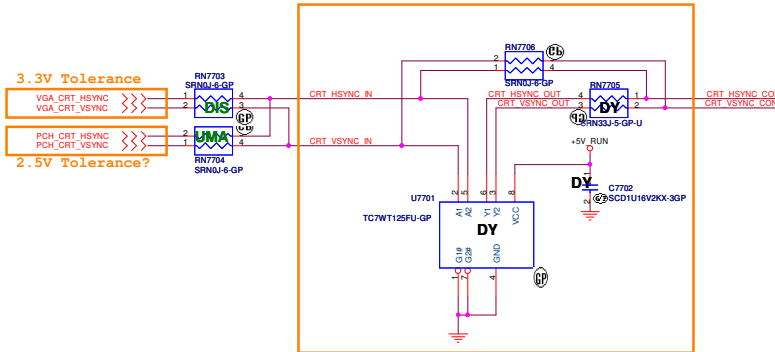


20.F0772.020
SEC. 20.F1035.020

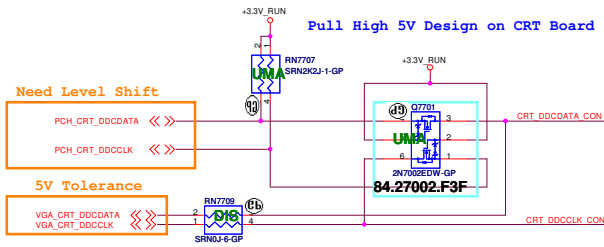
CRT RGB



CRT Hsync & Vsync level shift



CRT DDCDATA & DDCCLK level shift

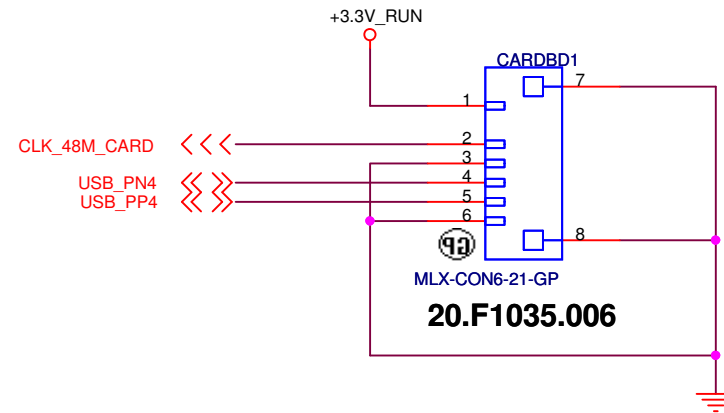


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Title CRT Board Connector			
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SSID = SDIO

Card Reader connector



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Title

CARD Reader CONN

Size
A4

Document Number

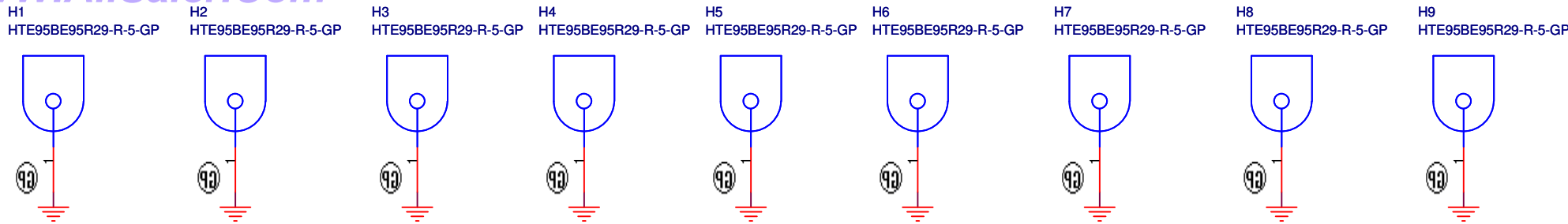
Berry

Rev

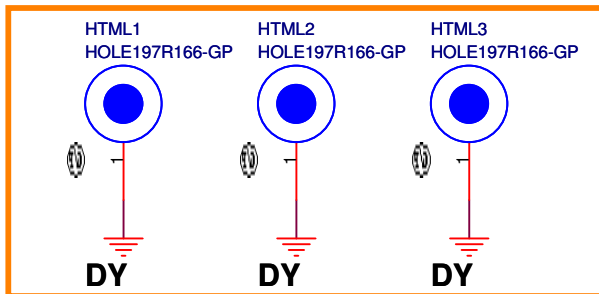
X00

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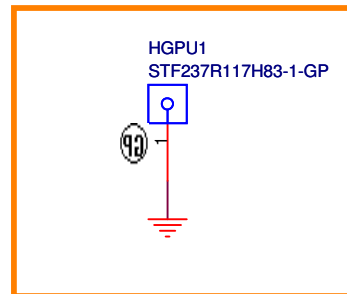
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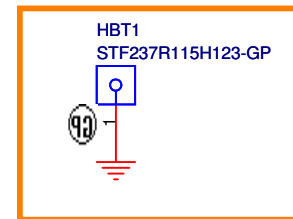
CPU Thermal module hole



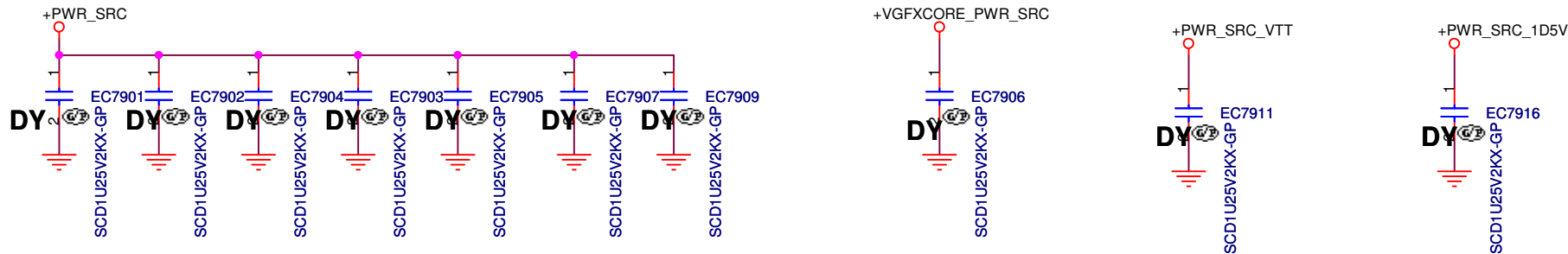
GPU Thermal module hole



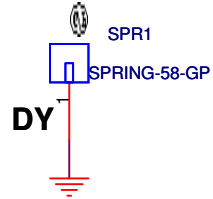
stand off



EMI Reserve



EMI Reserve



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Title

UNUSED PARTS/EMI Capacitors

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Document Number

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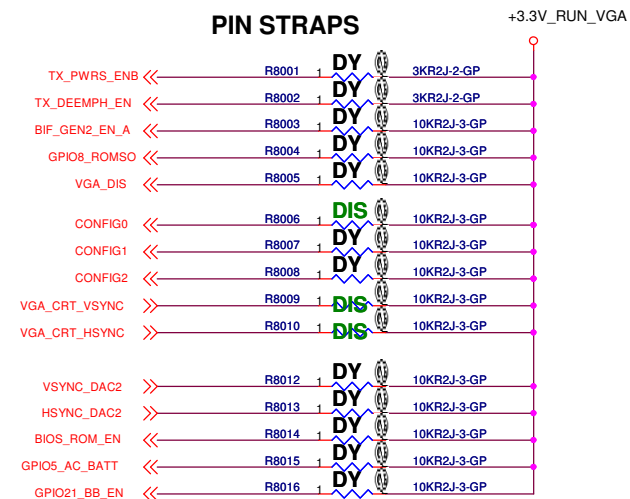
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ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

PIN STRAPS



<Core Design>



Title

GPU PCIE/STRAPPING(1/5)

Size

Document Number

Rev

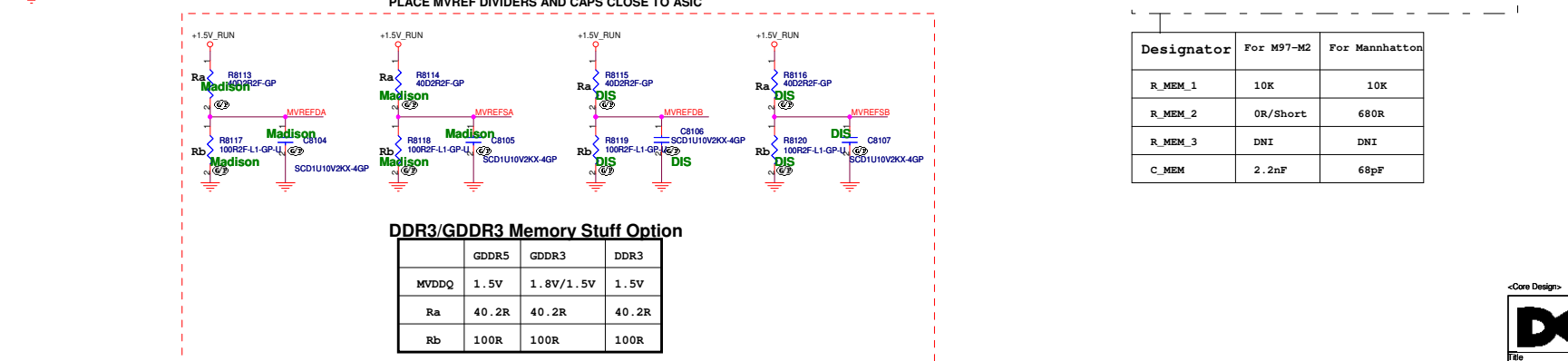
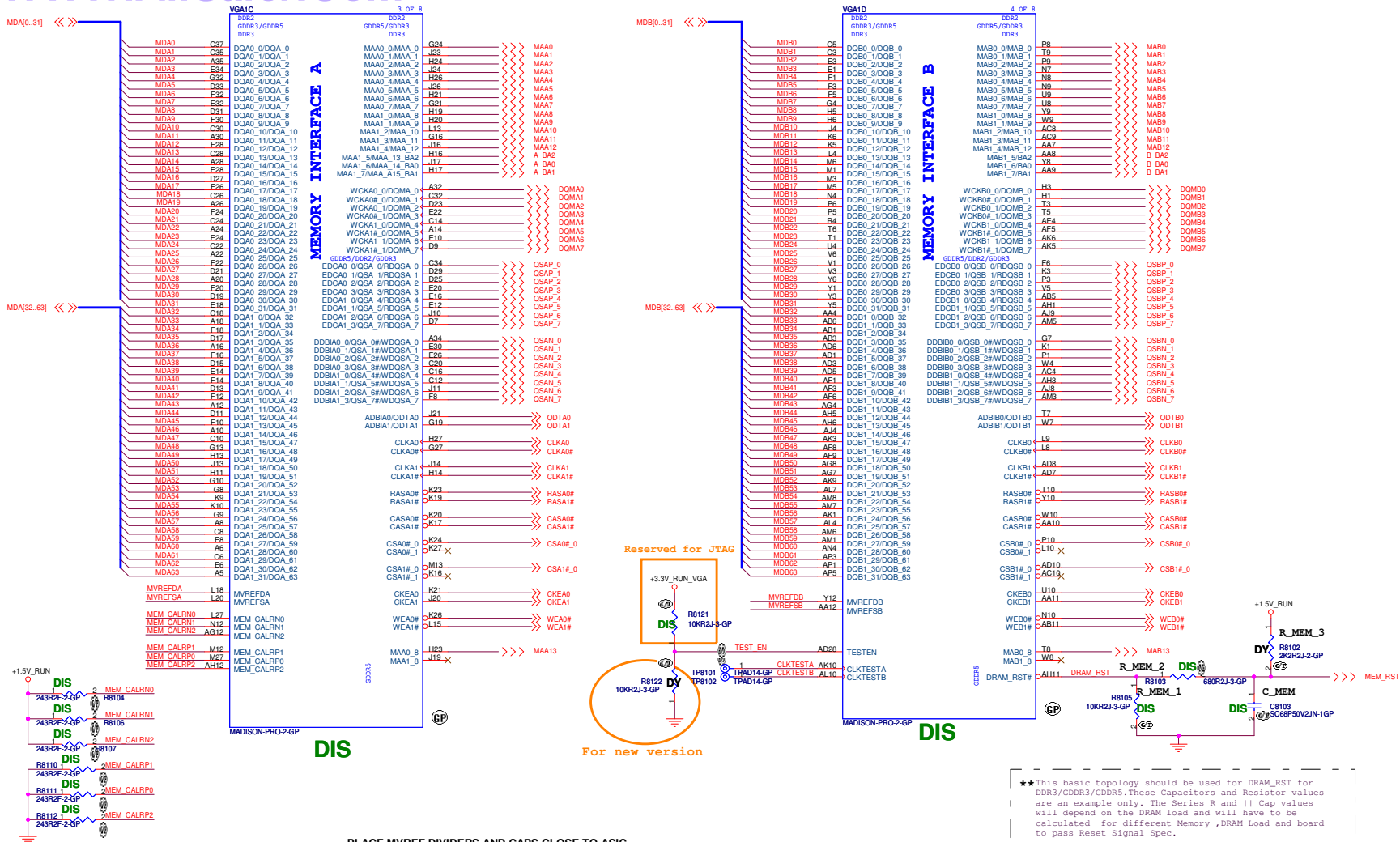
A3

Berry

X00

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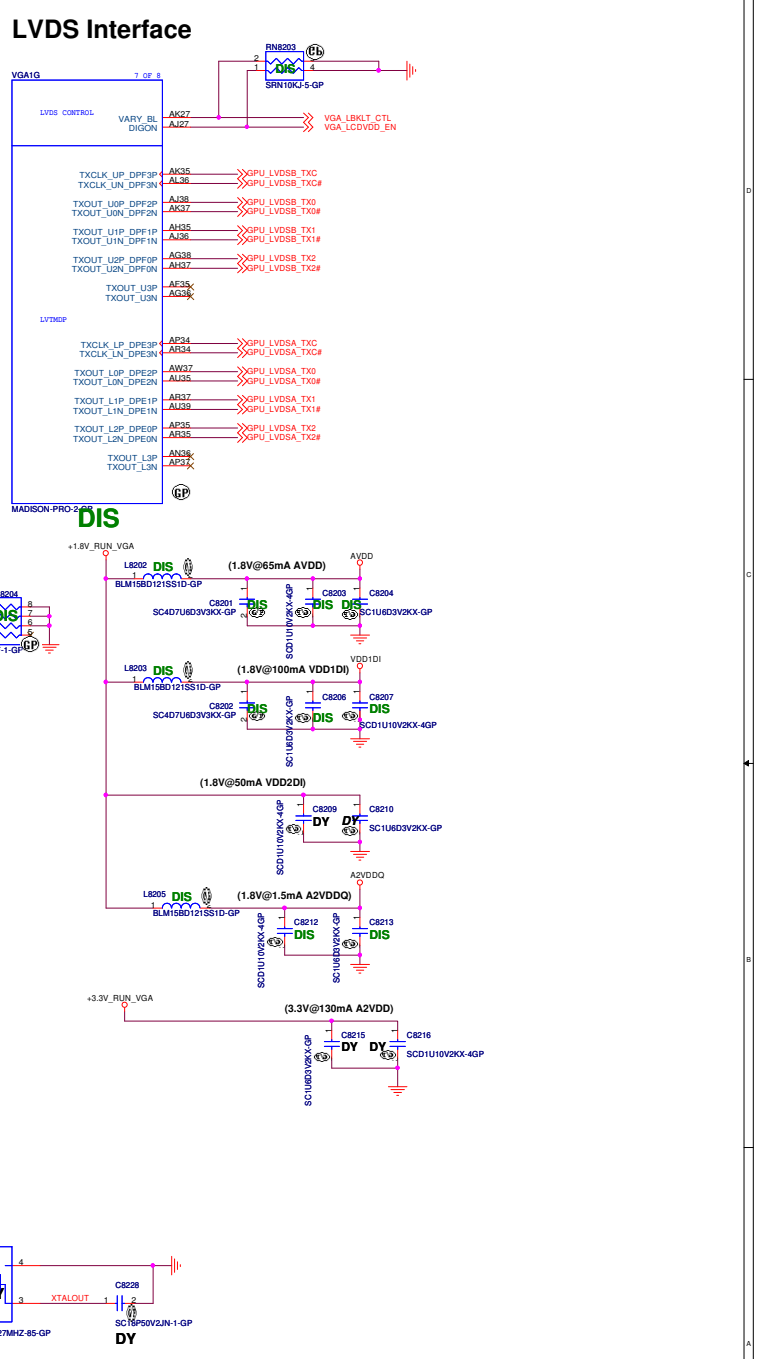
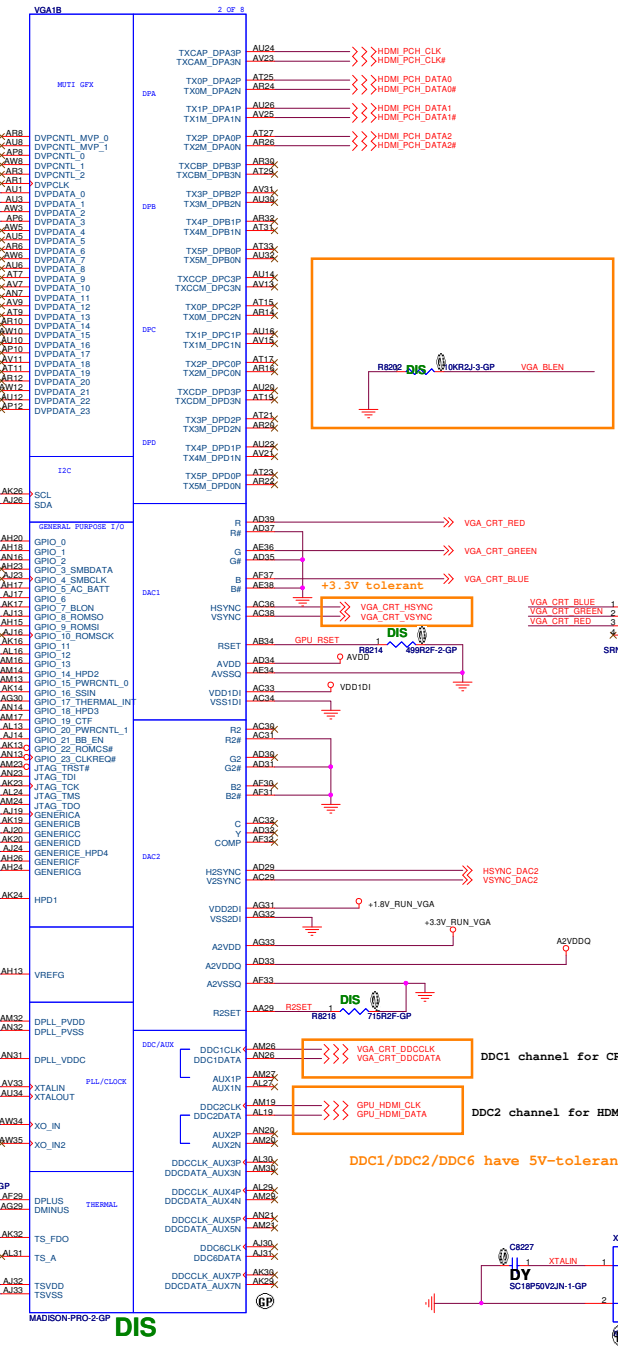
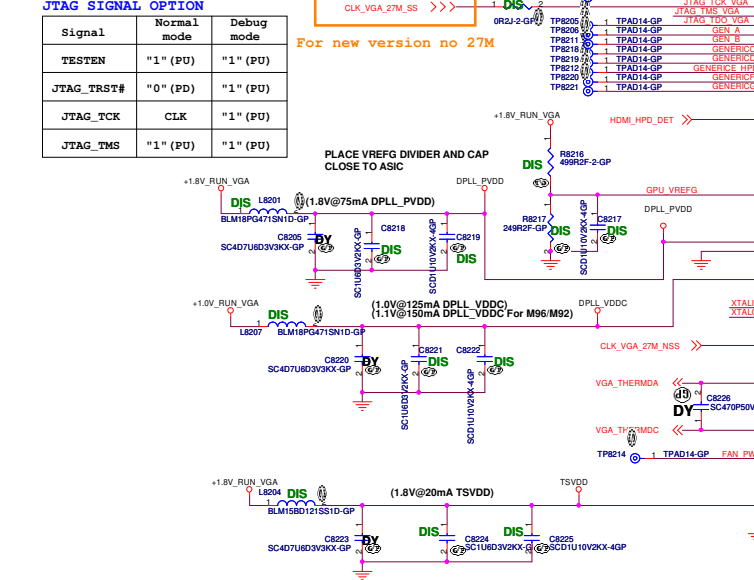
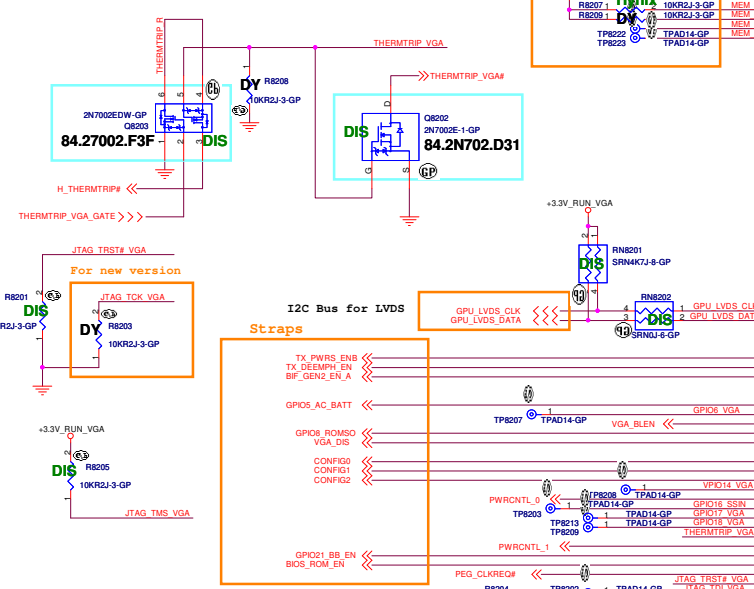


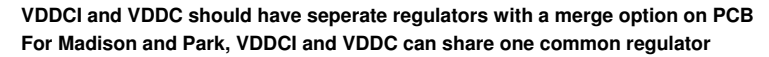
***This basic topology should be used for DRAM_RST for DDR3/GDDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and | Cap values will depend on the DRAM load and will have to be calculated for different Memory, DRAM Load and board to pass Reset Signal Spec.

MEMORY ID Table

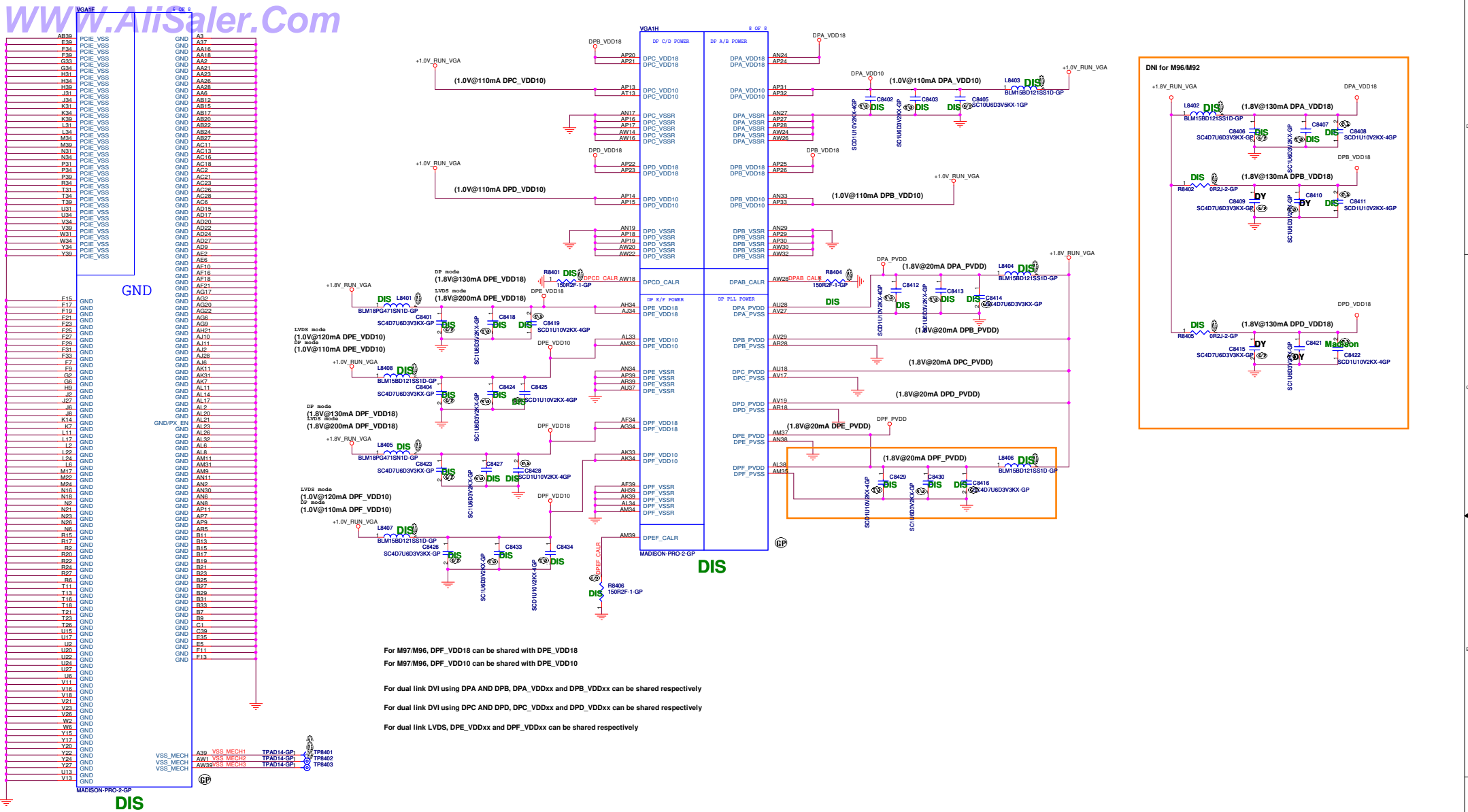
DVPDATA[0:3]	Description
1000	DDR3 Samsung-K4W1G1646E-HC12 (800MHz)
0000	DDR3 Hynix-H5TQ1G63BFR-12C (800MHz)

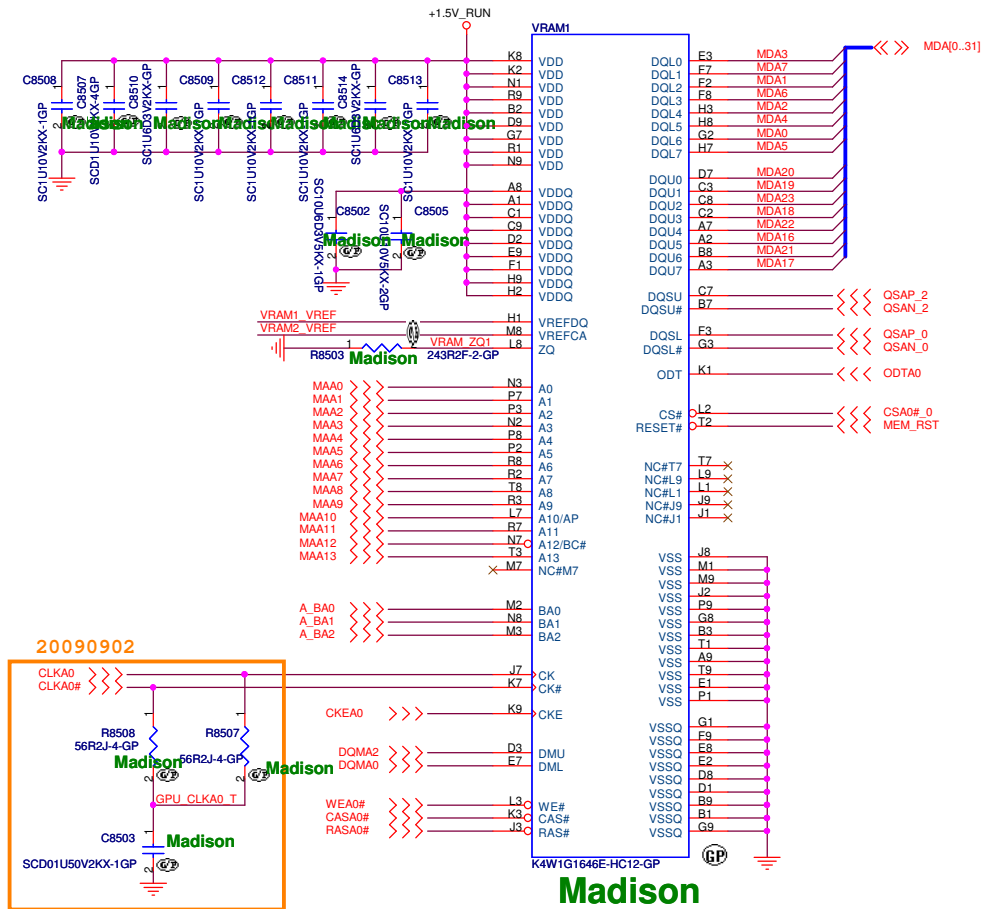
DVPDATA[0:3] Default: Pull down



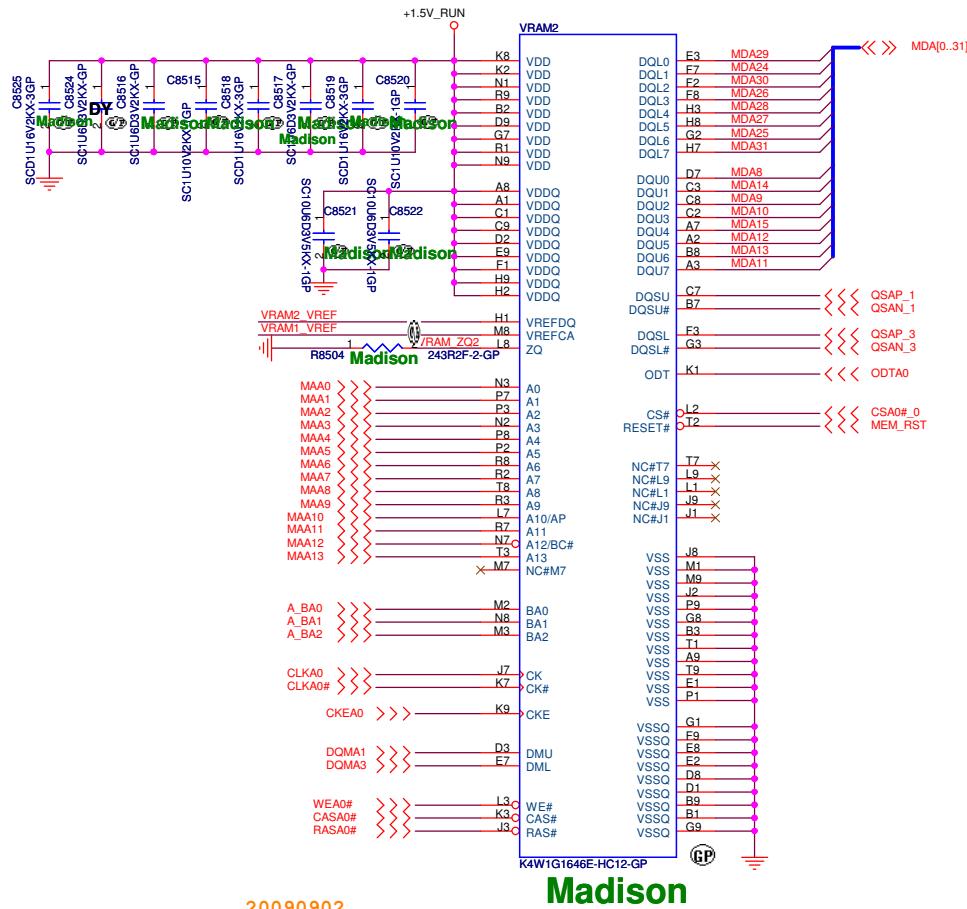


NOTE4:
For M2 design compatibility, refer to the document AN_M96_Ax and AN_M97_Ax

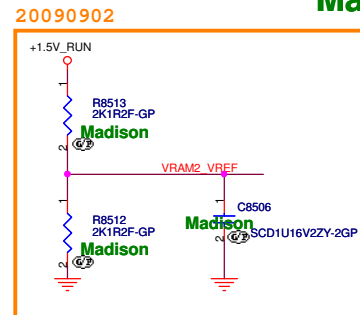
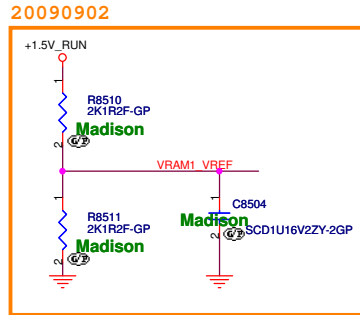


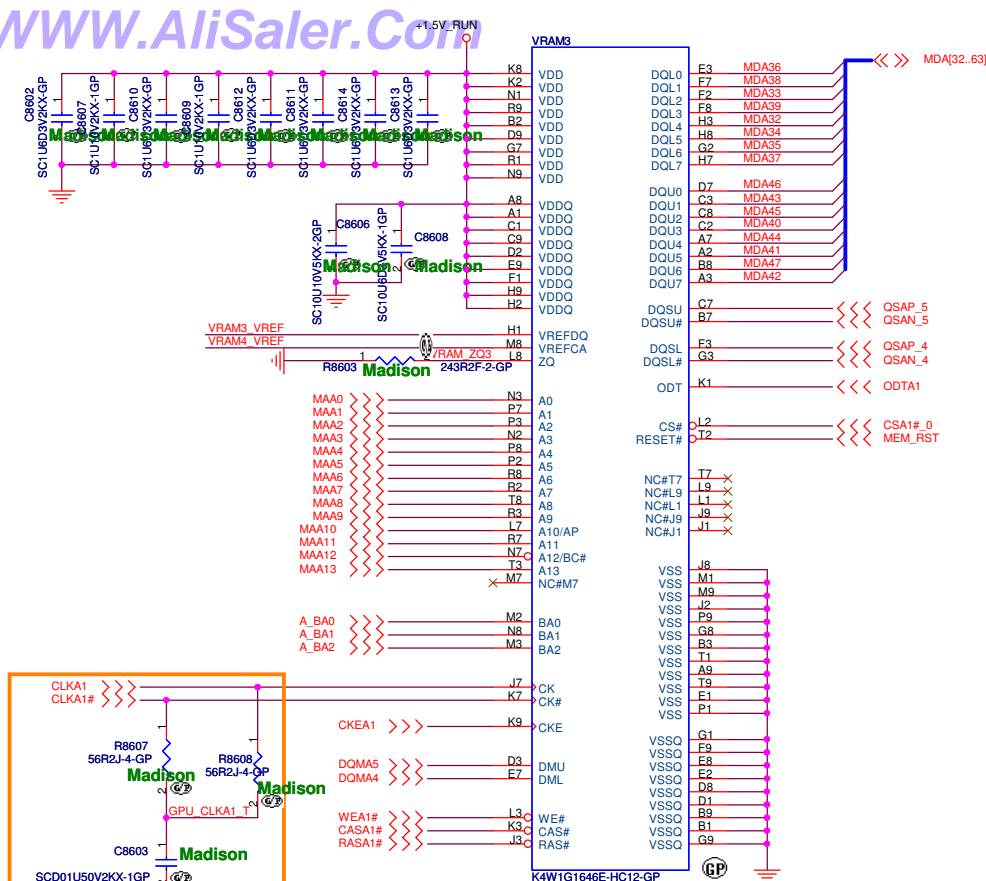


Madison



Madison

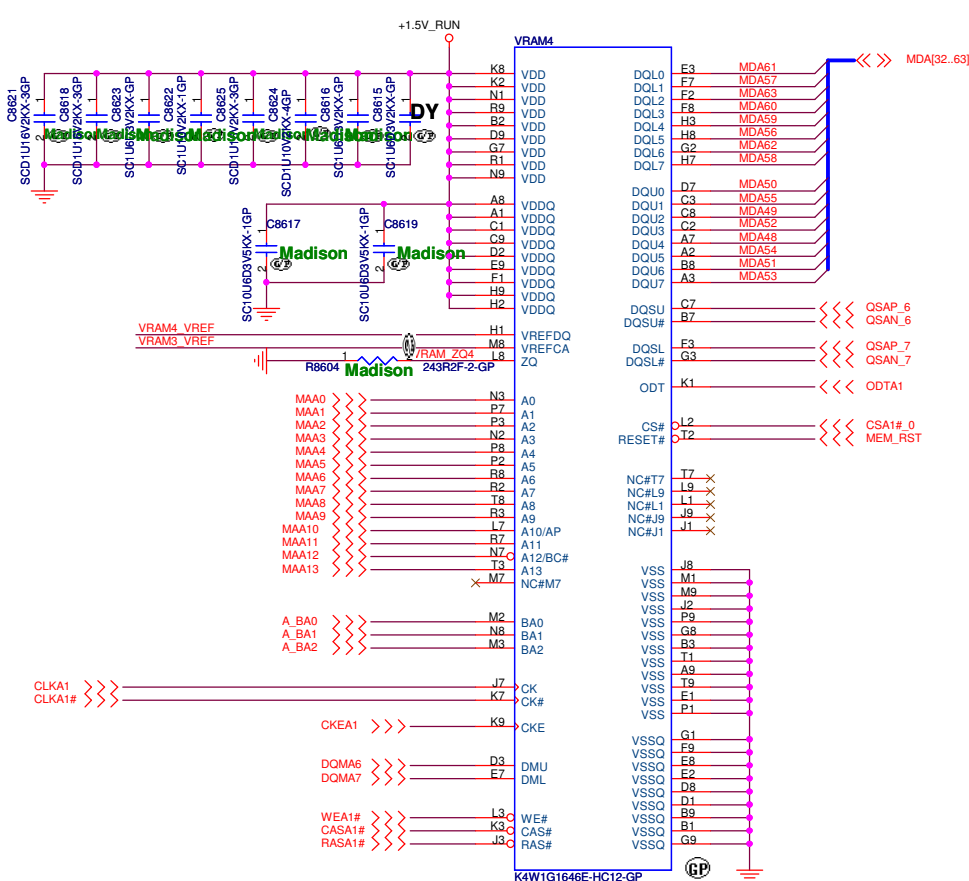
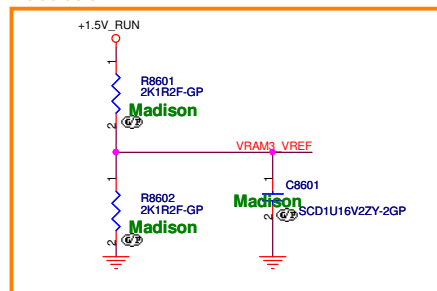




Madison

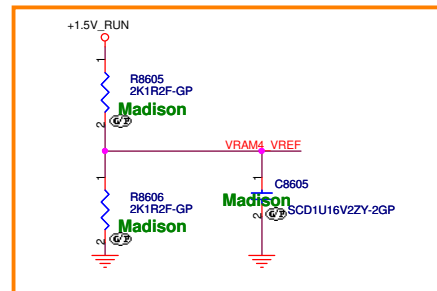
20090902

20090902

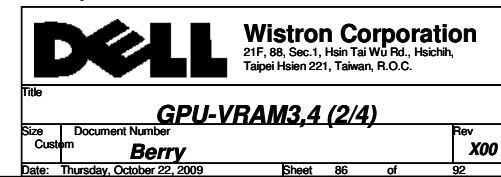


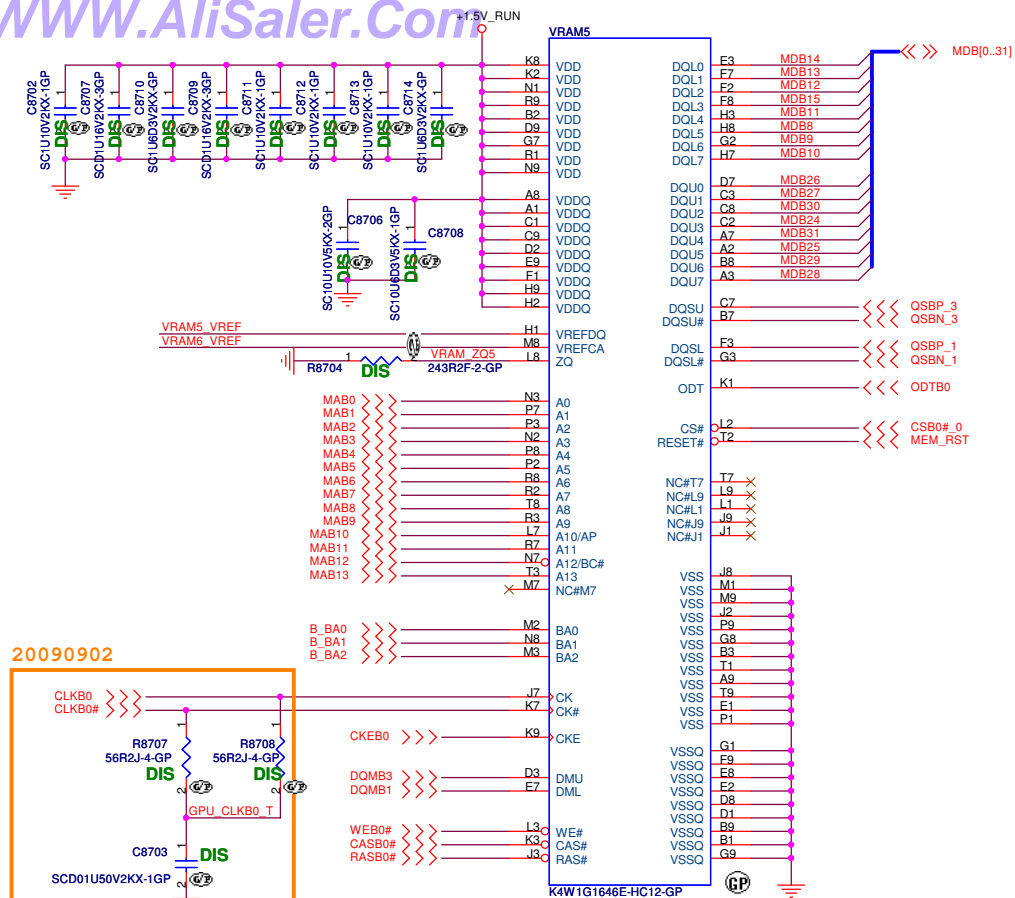
Madison

20090902

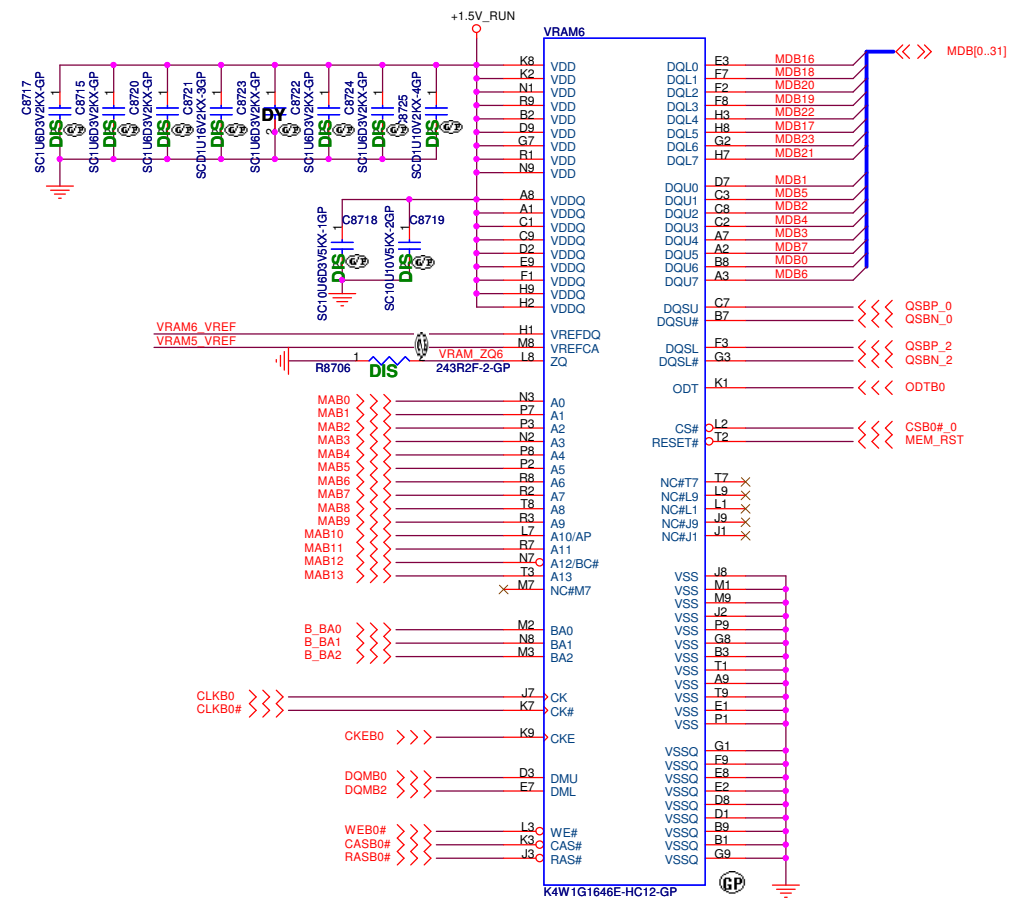
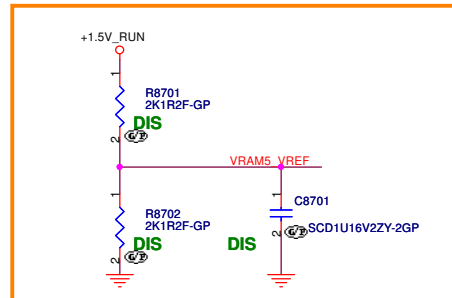


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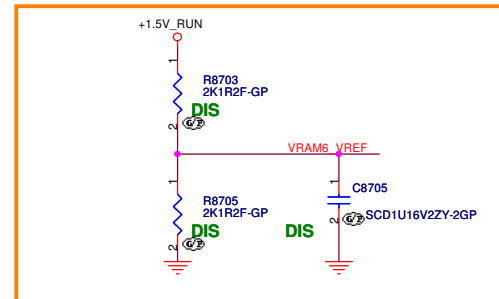




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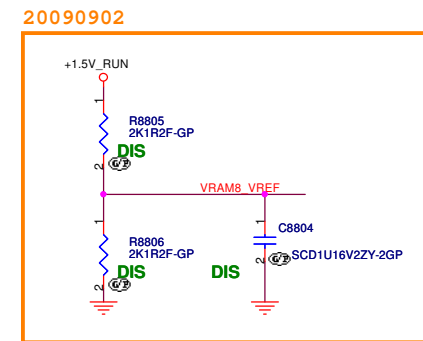
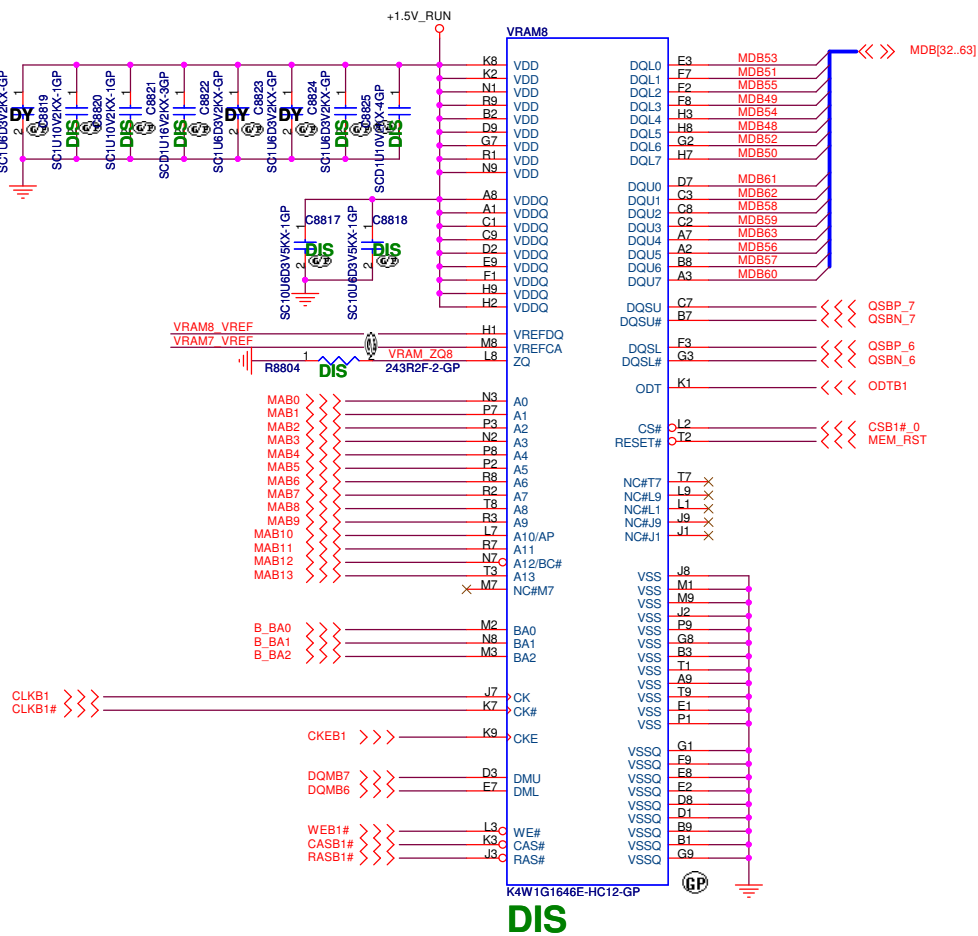
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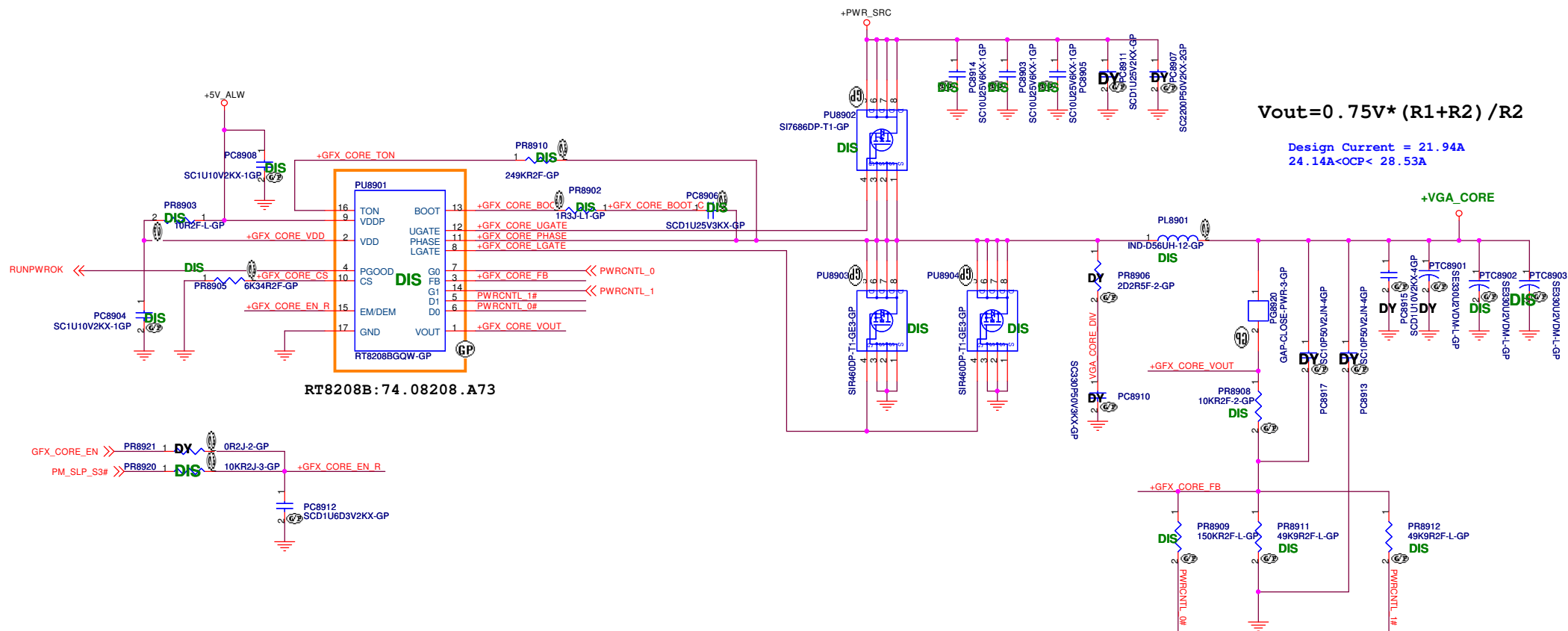


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PWRCNTL_0	PWRCNTL_1	+VGA_CORE
H	H	0.9V
L	H	0.95V
H	L	1.05V
L	L	1.1V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.6mohm/1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V PSLV0E337M(15) 15mOhm 2.886Arms NEC_TOKIN/ 77.C3371.10L
H/S: SI7686DP/ POWERPAK-8/11mOhm/14mOhm@4.5Vgs/ 84.07686.037
L/S: SI7460DP/ POWERPAK-8/ 4.9mOhm/6.1mohm@4.5Vgs/ 84.00460.037

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Title

RT8208B_+VGA_CORESize
A3

Document Number

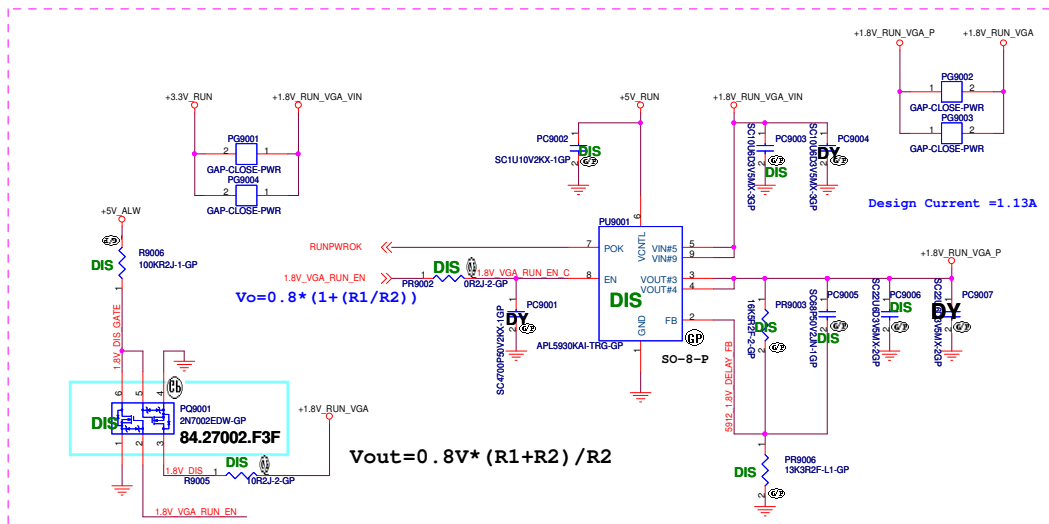
Arsenal DJ1 Discrete

Rev	X
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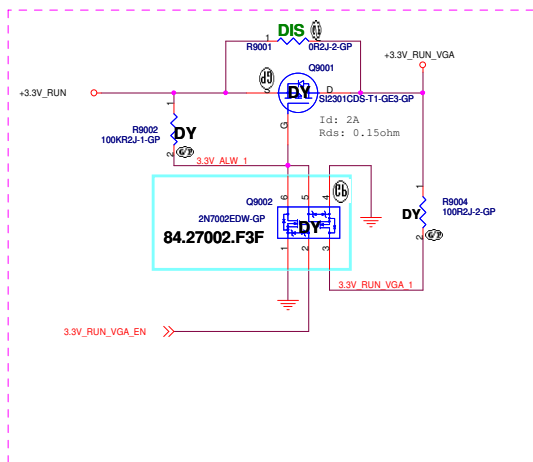
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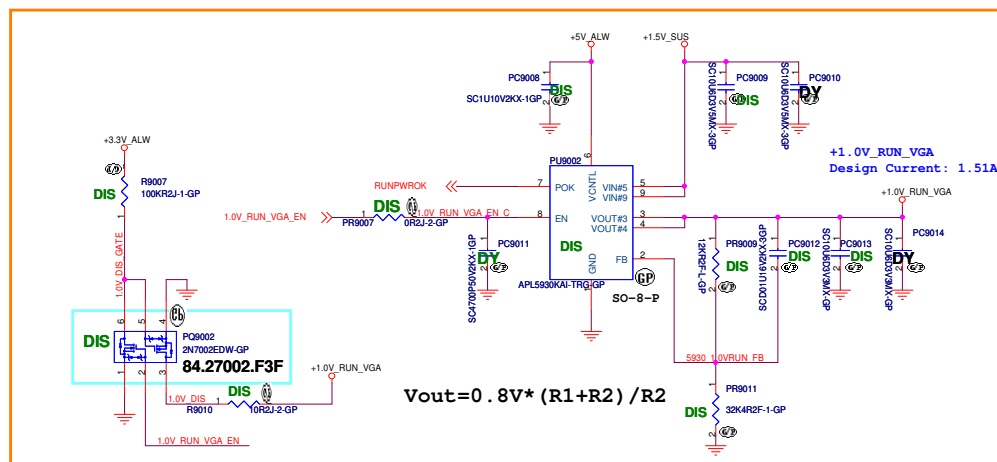
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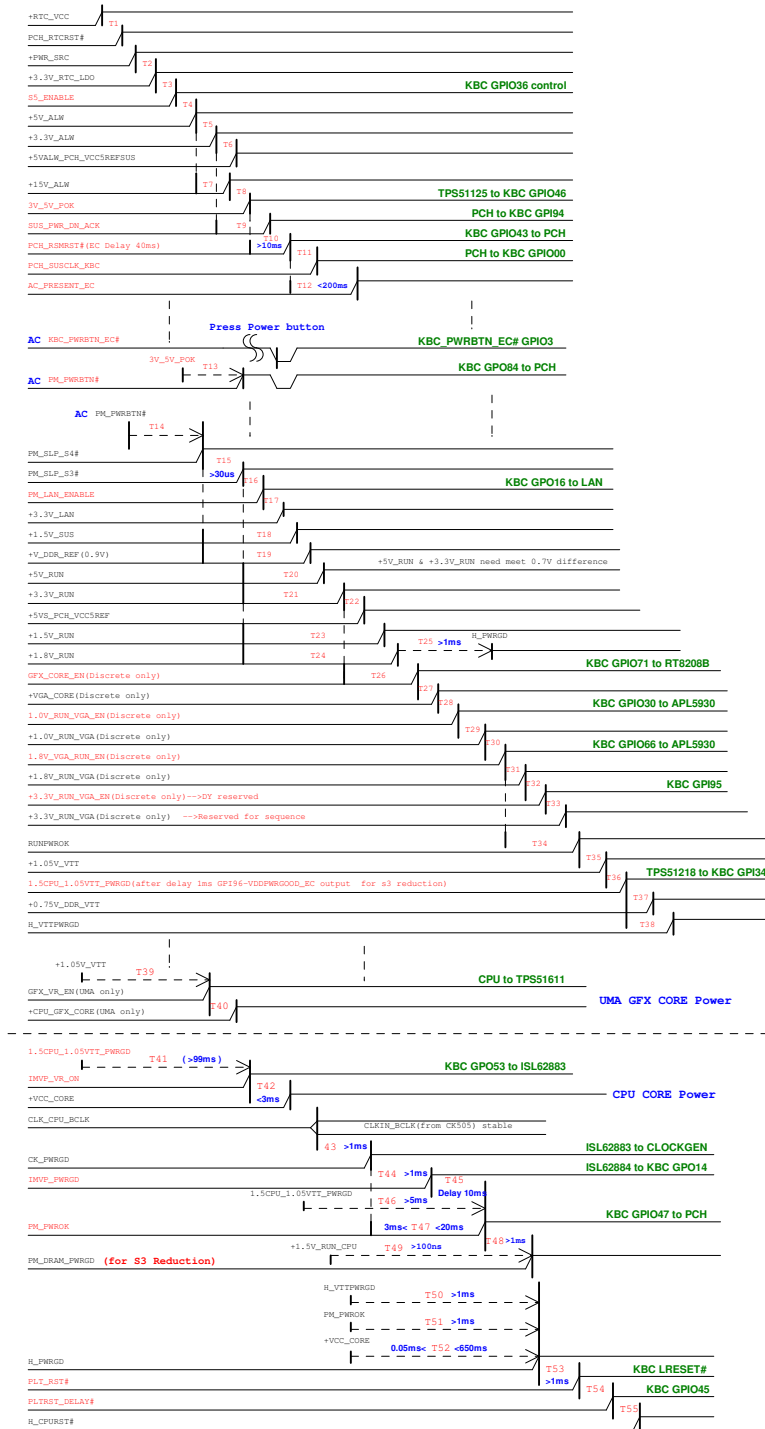
+3.3V_RUN_VGA



APL5930KAI for +1.0V RUN VGA

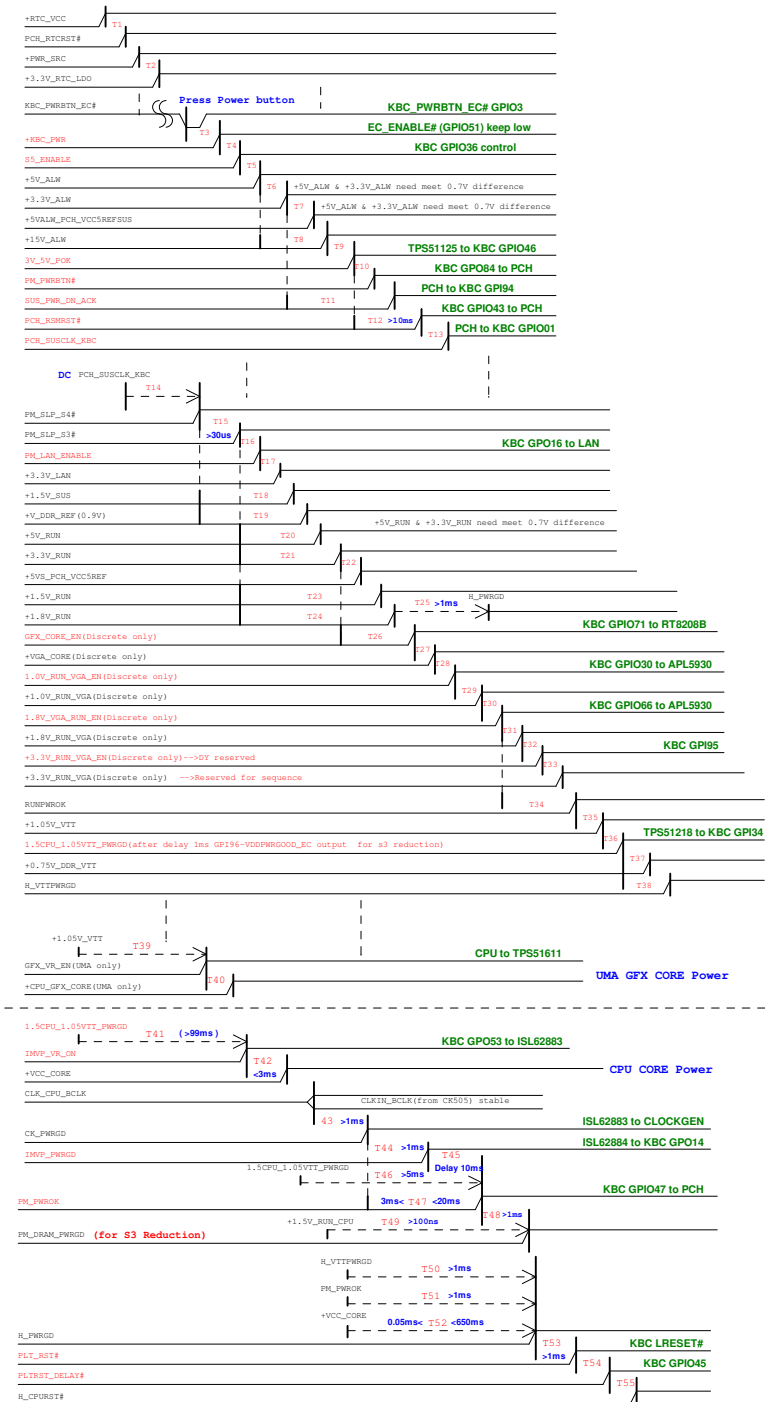


red word: KBC GPIC




(DC mode)

red word: KBC GPIO



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Title

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